H2020-MSCA-ITN-PETER. Proposal Number 812.790

Pan-**E**uropean **T**raining, research and education on **E**lectromagnetic **R**isk management (PETER)

Deliverable 3.1 – Integrated Circuit to measure absorbed energy

Authors:

Arunkumar Hunasanahalli Venkateshaiah

Dr. John F. Dawson

Dr. Martin Trefzer

Dr. Simon Bale

Department of Electronic Engineering, University of York, York, UK

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790

Deliverable Number	D3.1
Deliverable Name	Integrated Circuit to measure absorbed energy
Deliverable Duration	April 1, 2019 to March 31, 2020
Due Date of Deliverable	March 31, 2020
Actual Submission Date	March 31, 2020
Deliverable Lead Partner	University of York
Dissemination Level	Public
Work Package	WP3
No of Pages	
Keywords	IC, WP3

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

Table of Contents

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

Table of Figures

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

1. Introduction

This deliverable describes one of the key objectives of ESR9, to design Integrated Circuit (IC) to measure radio frequency energy absorbed into IC packages. Completing this objective unlocks the beginning of other objectives which allow us to verify and validate the probability of susceptibility of on-board electronic components.

Building on the power balance method developed by Hill [1] and Junqua [2], previous work at the University of York (UoY) has established that the energy absorbed in the contents of shielded enclosures must be known if the shielding effectiveness and internal fields are to be accurately determined [3]–[5]. This work focussed mainly on how much energy was absorbed into the contents (whole circuit boards) and its effect on the enclosure shielding effectiveness. In order to consider the susceptibility of electronic systems in this project, we planned to build an IC to measure the energy coupled into on-board ICs. This can then be coupled with the IC-EMC methodology developed by Ramdani, Sicard, et al [6] to assess the risk of susceptibility to EMI of ICs on a circuit board in a system.

From our previous work [7], [8], we have a methodology to estimate the power coupled into the loads of a PCB trace. As part of the PETER project, we aim to produce an IC that can be used to monitor power coupled into an IC pin, so that the power coupled into the IC itself can be measured. This will allow us to validate a susceptibility prediction methodology. Figure 1 illustrates how the Detector IC might be used on a test PCB. Test tracks of different geometries are coupled to the Detector IC, and energy will be coupled to the test tracks either via connectors or electromagnetically in a reverberation chamber. The RF levels detected are relayed to external instrumentation via a microcontroller and communications IO interface. The microcontroller will also provide control signals to the detector IC.

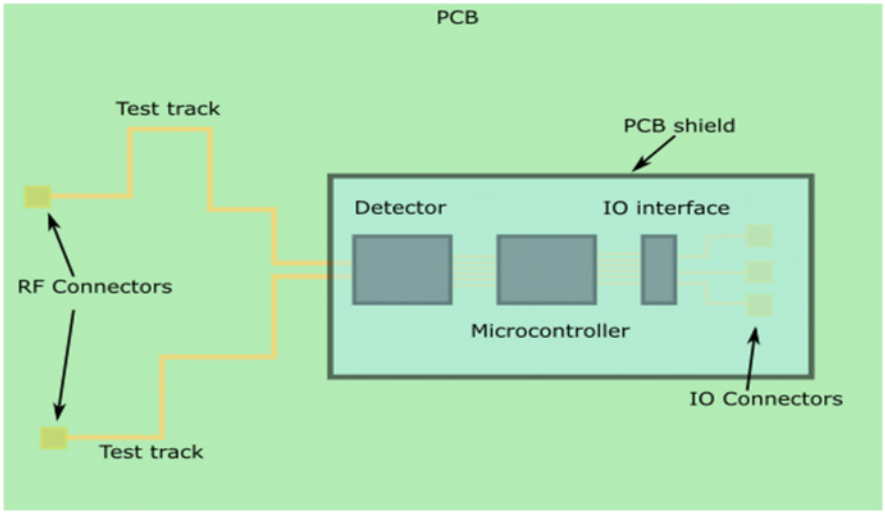

Figure 1: PCB Concept

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

1.1 IC Detector Block Diagram

The IC Detector will incorporate eight detector channels connected to package pins in the numbered as channels zero to seven as shown in Figure 2. Channels 0-3 have different sensitivity levels based on the amplification circuit blocks used in them, channels 4-7 have identical input circuits to the channels 0 to 3. The only difference is that channels 0 to 3 have low series resistance (<1 Ω) analogue input I/O cells whereas channels 4-7 have 100 Ω series resistance analogue input I/O cells. Each set of channels connect via an analogue multiplexer to a differential instrumentation amplifier (IA) and then to a high series resistance (1k Ω) analogue output I/O cell.

Channels 0 and 4 contain a high gain RF amplifier which helps to maximise the level of sensitivity of the detector. Channels 1 and 5 incorporate broadband RF amplifier which helps the detector to operate slightly for the higher frequency band with reduced sensitivity. Channels 2 and 6 do not have any amplification and the input signal is directly connected to the Peak Detector (PD). For channel 3 and channel 7 the input signal is directly fed to IA.

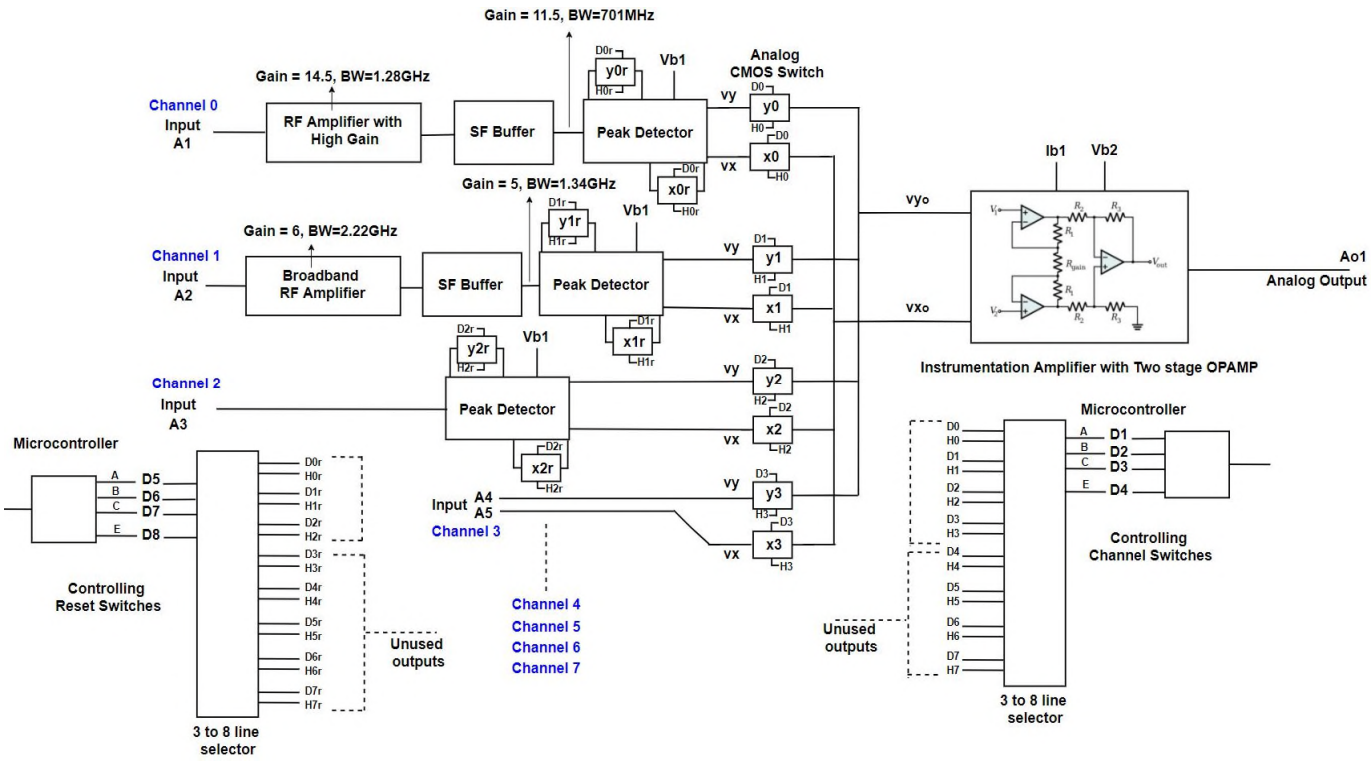

Figure 2: IC Detector Block Diagram

The channels are switched using analogue CMOS switches which are controlled by a 3 to 8-line decoder. Channels 0 & 4 operate simultaneously since their switches are connected to the same output pins of the decoder. Similarly, channels 1 & 5, 2 & 6, and 3 & 7 are connected to the same output pins of the decoder respectively for simultaneous operation. However, channels 0 to 3 and channels 4 to 7 have different outputs connected through different IA. A

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

similar control operation is employed for the switches used to reset the PD's capacitor. The control signals for 3 to 8-line decoder are given from the external microcontroller.

2. Design and Layout of Each Circuit Block

1.2 RF Amplifiers

The RF amplifiers use the cascode technique which is very common in improving analogue circuit performance. The RF amplifiers (Figure 3 and Figure 6) use a two-stage cascode circuit that employs CS-CG (Common Source Common Gate) configuration. The common source amplifier is used as the input stage driven by an external signal source, whereas the common gate amplifier is used as the output stage.

All the designs are carried out using X-FAB XT018 0.18u HV SOI CMOS technology in Cadence Simulator.

1.2.1 High Gain RF Amplifier

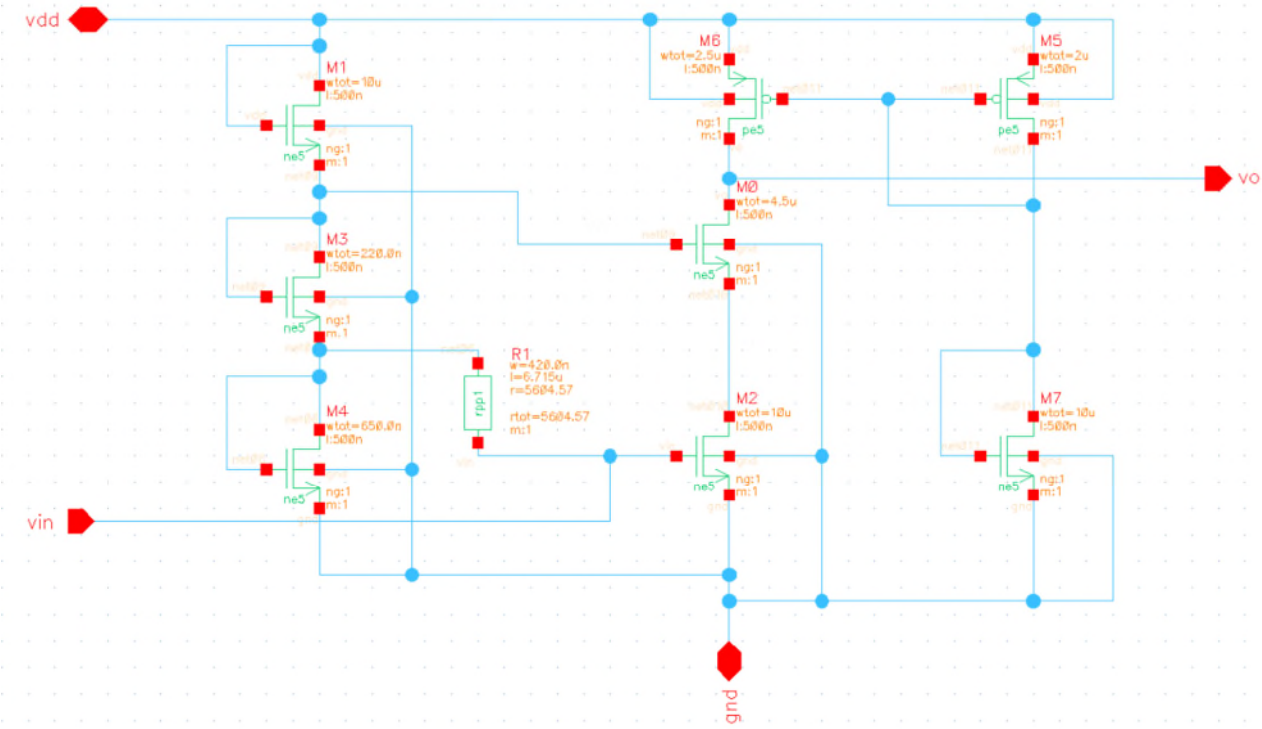

Figure 3: High Gain RF amplifier Schematic

In the cascode configuration, MOSFET 2 (M2) is the common source amplifier and M0 is the common gate amplifier. A cascode amplifier needs a high impedance load to obtain a high gain [9]–[11]. Hence, the PMOS current mirror (M6 and M5) is used as the load for the RF amplifier. The small-signal output resistance of the common gate amplifier (M0) and the small-signal resistance of the current mirror (M6 and M5) can be varied to achieve a high gain bandwidth product. By varying the width of the MOSFET M0 and M6, a high gain can be achieved by giving up some bandwidth as a trade-off.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

MOSFETs M1, M3 and M4 are used as a voltage divider to provide different bias points for the gate of the common source amplifier M2 and gate of the common gate amplifier M0.

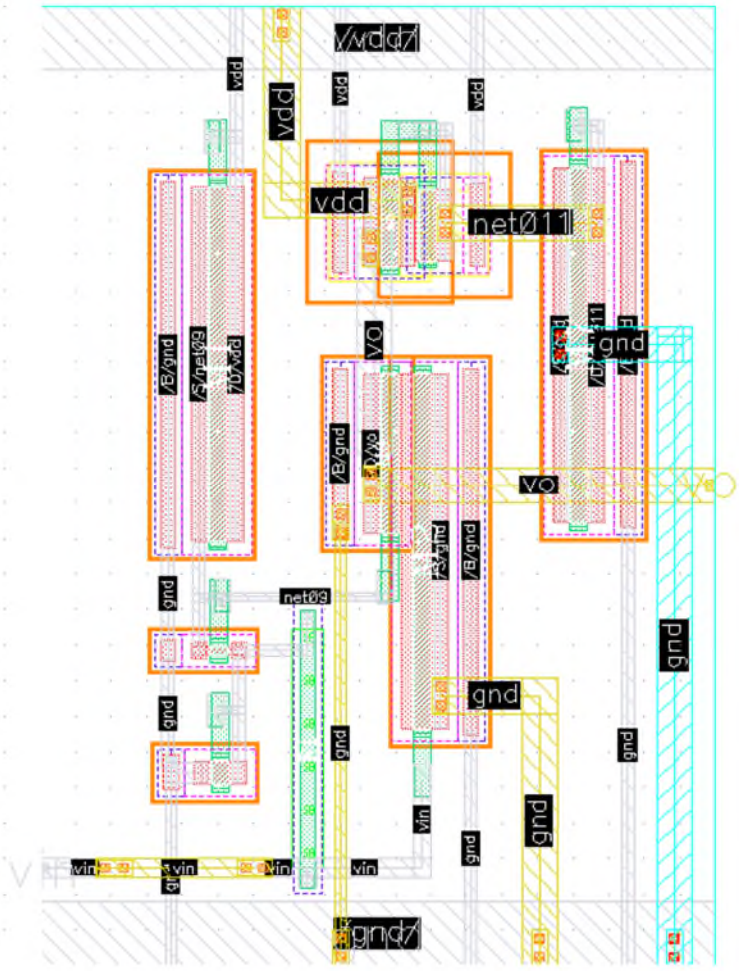

Figure 4: High Gain RF amplifier Layout

Figure 4 shows the layout design of the high-gain RF amplifier. The frequency response of the high gain RF amplifier is as shown in Figure 5. The red curve shows the schematic simulation results, whereas the yellow line shows the post-layout simulation results. VDD=5V, for the entire design.

Schematic results have a gain of 23dB and a bandwidth of 1.28 GHz. Whereas post-layout simulation results show the gain of nearly 23dB and bandwidth of 991.77 MHz as shown in Figure 5. The reduction in bandwidth is due to additional parasitic resistance and capacitance of the interconnect included in post layout simulation.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

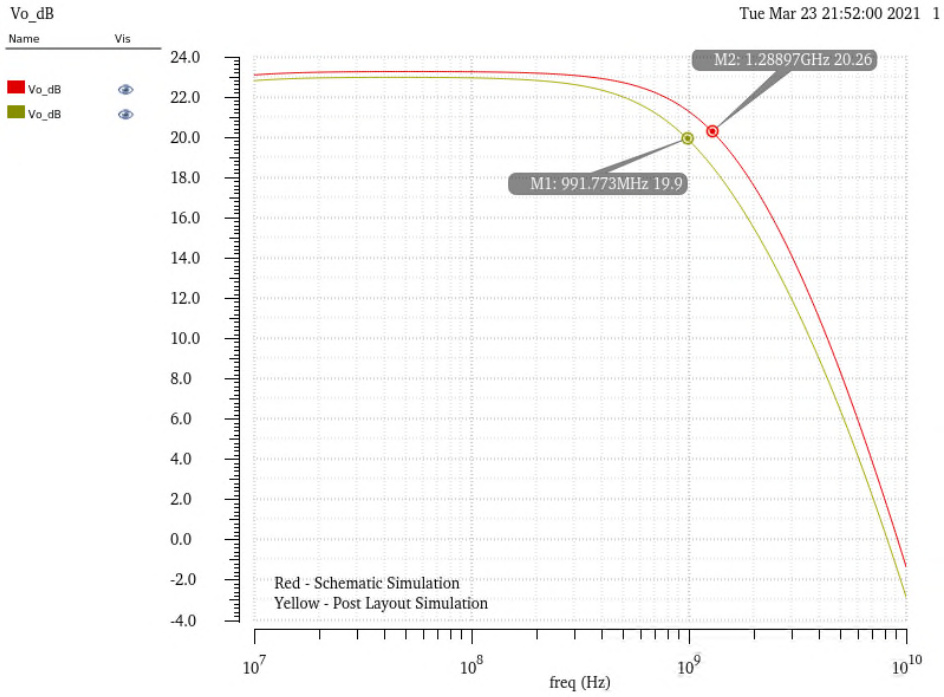

Figure 5: Frequency Response of Schematic (red) and Post Layout (yellow) Simulation with 1.20GHz RF amplifier: 991.77 MHz (23dB).

1.2.2 Broadband RF Amplifier

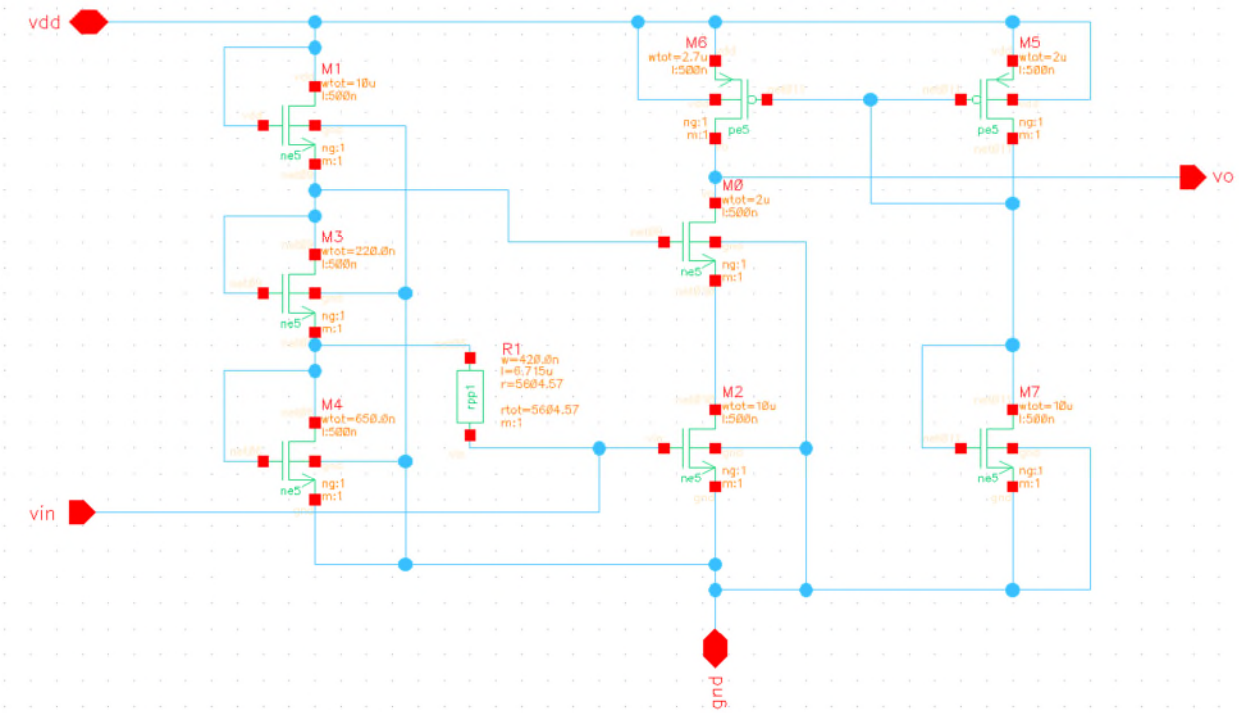

Figure 6: Broadband RF amplifier Schematic

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

The design of the broadband RF amplifier shown in Figure 6 remains almost the same as the high gain RF amplifier. The only difference is, that in order to achieve high bandwidth the width of the MOSFET M0 and M6 is modified.

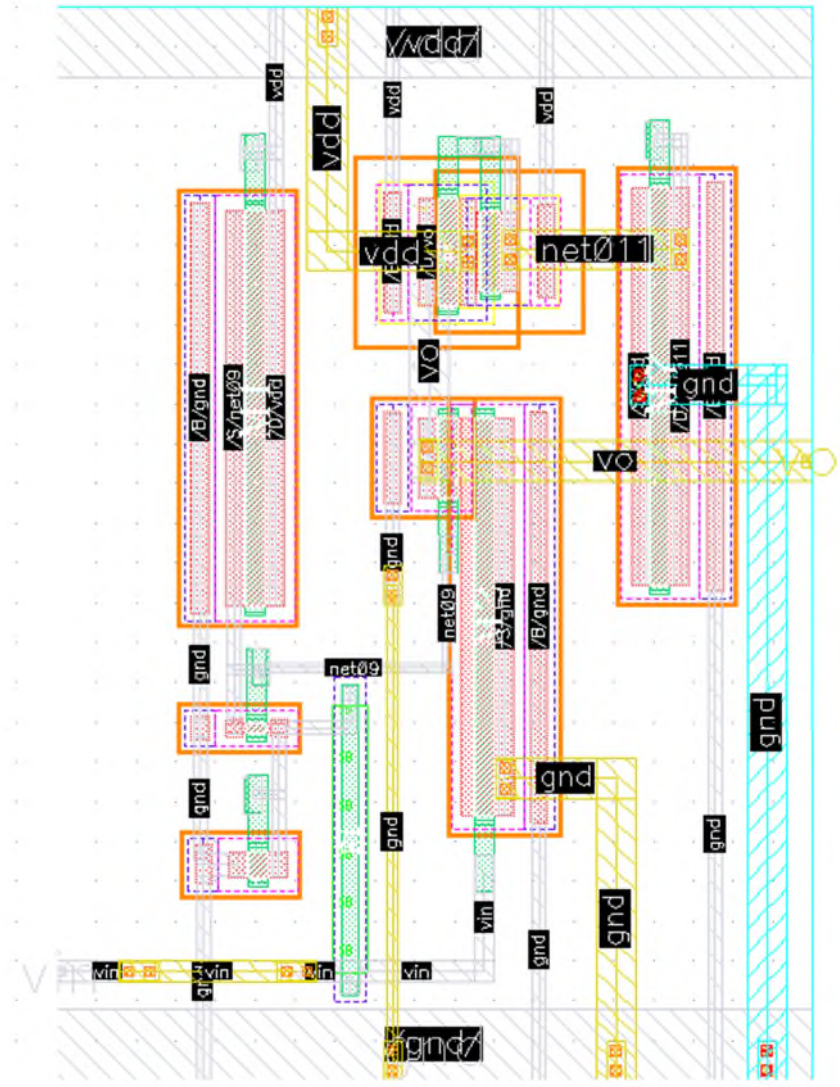

Figure 7: Broadband RF amplifier Layout

Figure 7 shows the layout design of the high-gain RF amplifier. The frequency response of the high gain RF amplifier is as shown in Figure 8. The red curve shows the schematic simulation results, whereas the yellow line shows the post-layout simulation results.

Schematic results have a gain of 15.5dB and a bandwidth of 2.25 GHz. Whereas post-layout simulation results show the gain of nearly 15.5dB and bandwidth of 1.92 GHz as shown in Figure 8. The reduction in bandwidth is due to additional parasitic resistance and capacitance of the interconnect included in post layout simulation.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

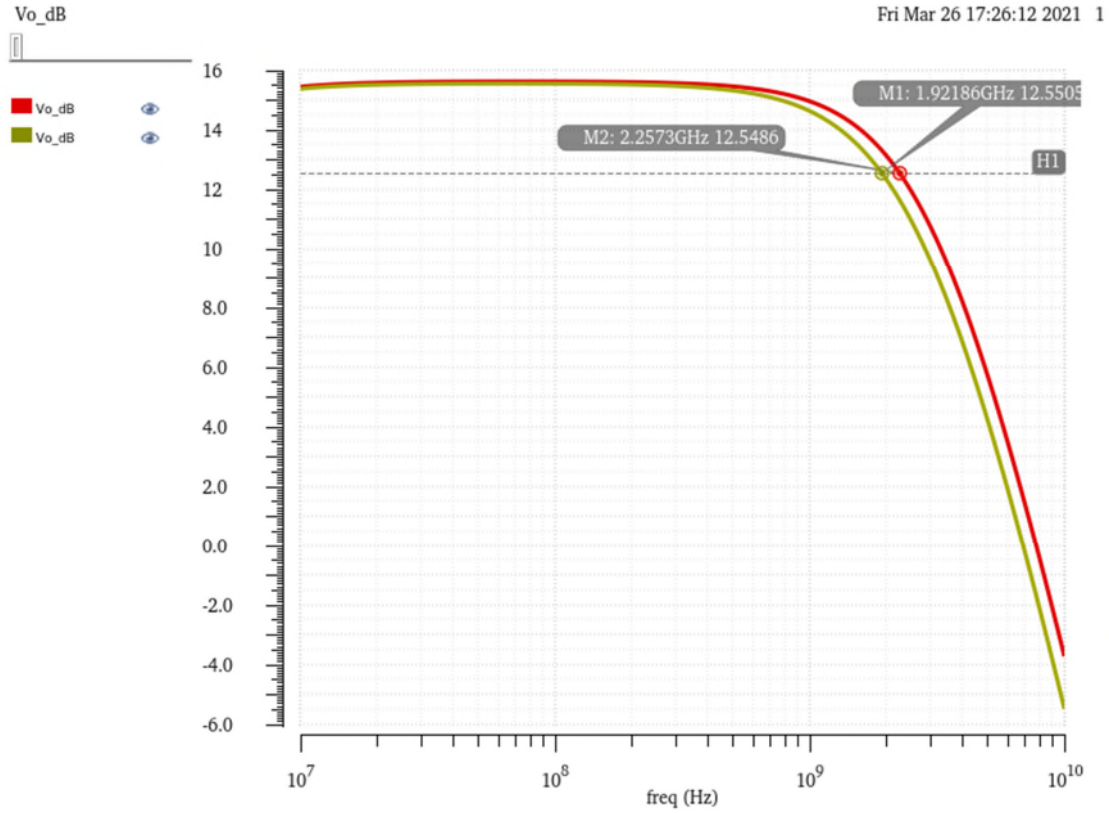

Figure 8: Frequency Response of Schematic (red) and Post Layout (yellow) Simulation with 2.25GHz RF amplifier: 1.92 GHz (15.5dB).

1.3 Source Follower Buffer

The source follower (SF) is a common-drain configuration, which is typically used as a voltage buffer. Common-drain configuration circuits are called followers because output voltage follows the input voltage. A source follower provides high input resistance, low output resistance, and inherently infinite current gain [9]. This circuit block will help to prevent the rf amplifiers being loaded by the detector.

Due to the lower transconductance of MOSFET compared to BJT transistors, comparatively the gain is not very close to unity [9]. However, for our application, the gain we are getting is close enough to unity gain as shown in Figure 11.

MOSFET M0 is of common-drain configuration and MOSFET M2 & M3 are the current mirror used to bias the transistor M0 as shown in Figure 9.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

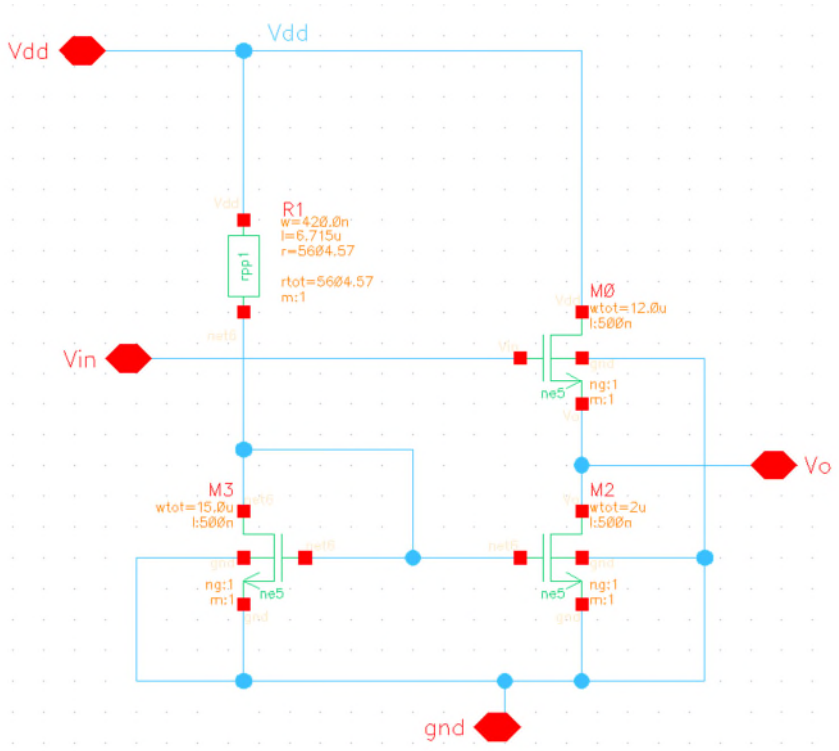

Figure 9: Source Follower Schematic

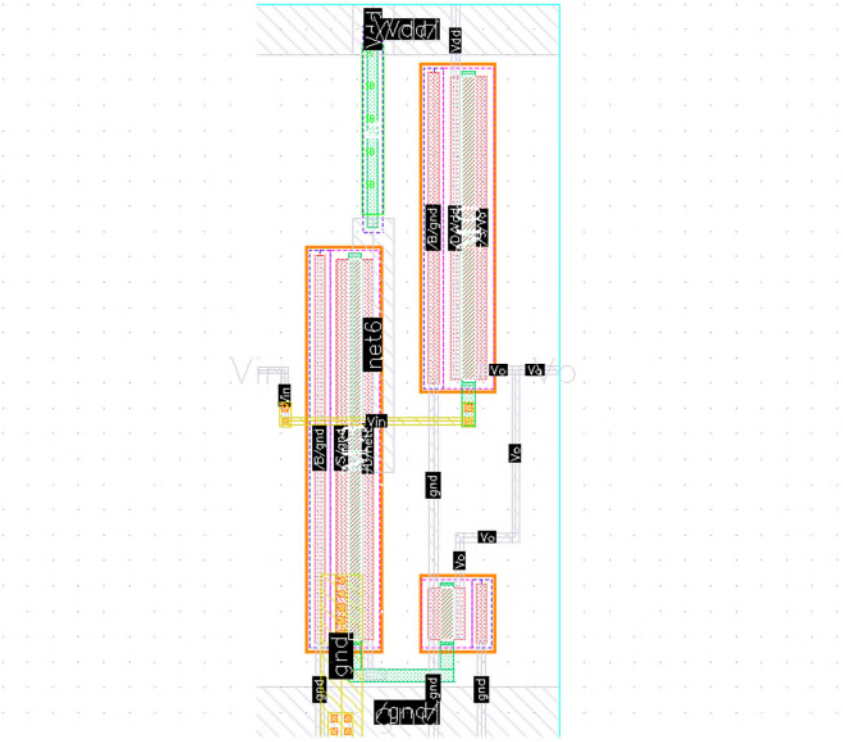

Figure 10: Source Follower Layout

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

Figure 10 shows the layout design of the source follower amplifier. The frequency response is as shown in Figure 11. The yellow curve shows the schematic simulation results, whereas the red line shows the post-layout simulation results.

Both schematic and post-layout simulation results have a gain of -1.6dB. Whereas the bandwidth for schematic simulation is 7.87 GHz and for the post-layout simulation is 6.59 GHz as shown in Figure 11.

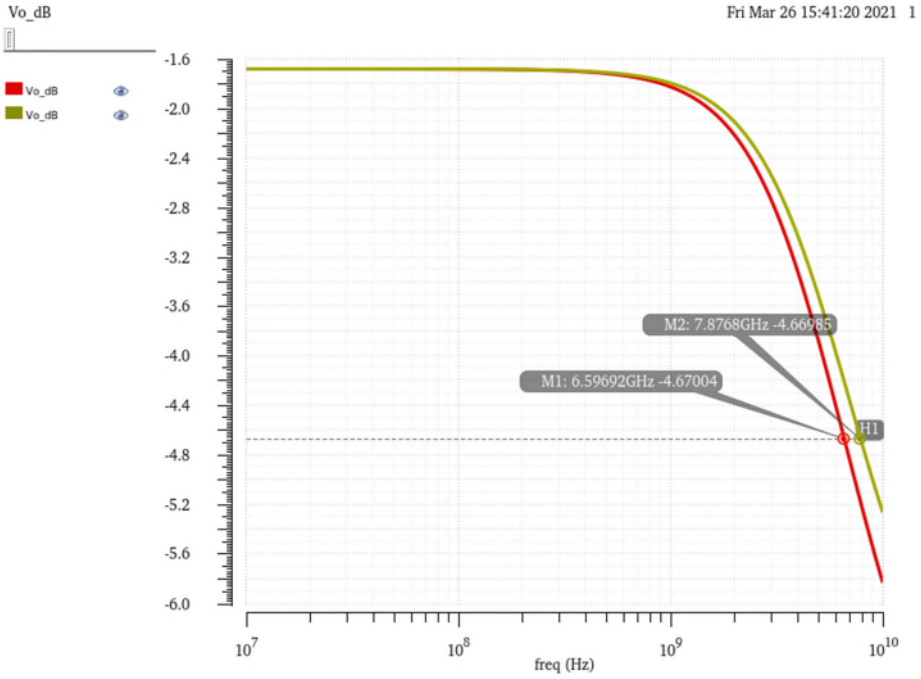

Figure 11: Frequency Response of Source Follower, which has a gain of nearly unity -1.6dB

1.4 Peak Detector

There are several ways to design a peak detector (PD). The simplest method is to design using a diode and capacitor. Usually, a resistor is used to discharge the capacitors in practical applications, however for our application, we use an analogue reset switch (not shown here) to discharge the capacitor. As the name suggests, the peak detector detects the peak of the analogue signal and holds the voltage till the capacitor is discharged through the reset switch.

Diode D0 and capacitor C0 show the simple peak detector configuration as shown in Figure 12. In order to compensate the diode drop at the output of the peak detector from D0, another dummy peak detector is connected opposite to it, which makes the differential output of Vx and Vy free from diode drop. Resistor R0 provides a dc current path to charge the capacitor.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

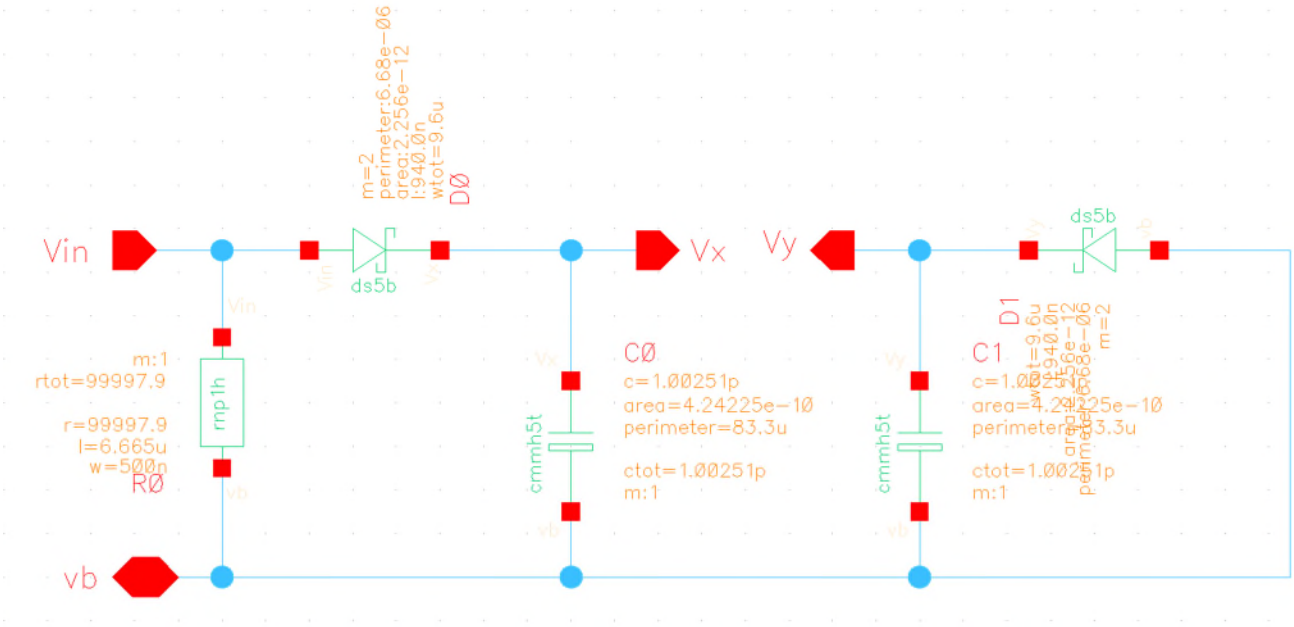

Figure 12: Peak Detector Schematic

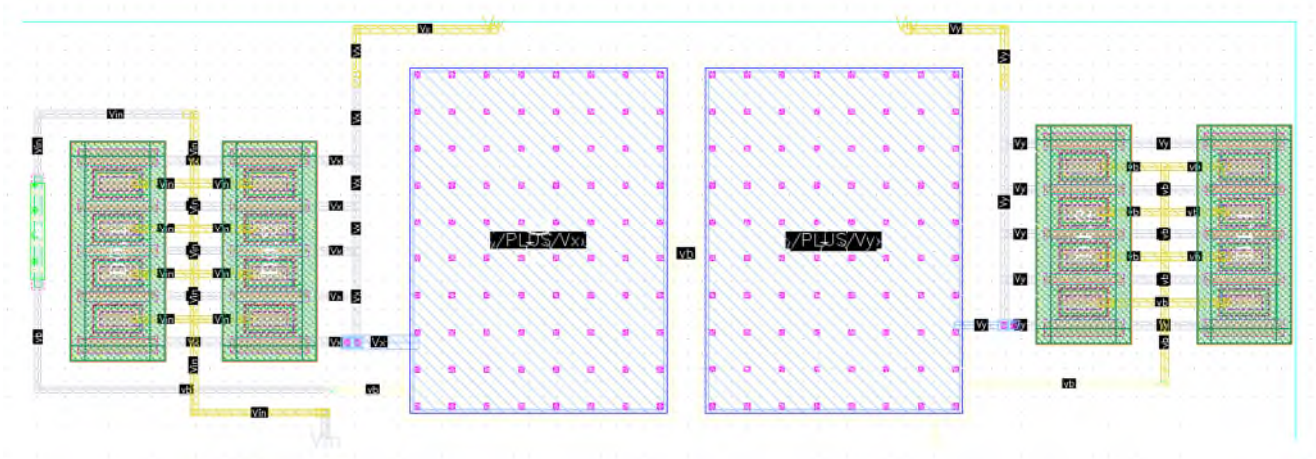

Figure 13: Peak Detector Layout

Figure 13 shows the layout design of the peak detector. To run the post-layout simulation in Cadence simulator a connection between ground and substrate must be initiated, which is only possible with active devices. Since our peak detector comprises only passive devices and does not have any active devices, an active device circuit block is necessary to run the post-layout simulation. Hence, a source follower circuit is used to drive the peak detector circuit as shown in Figure 14 (schematic) and Figure 15 (layout) to compare the schematic results and the post-layout simulation results.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

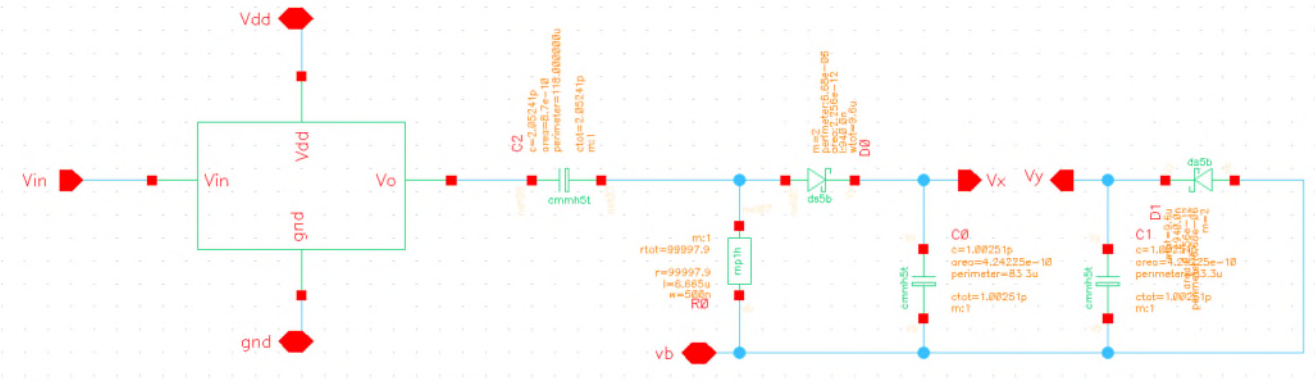

Figure 14: Source Follower together with Peak Detector Schematic

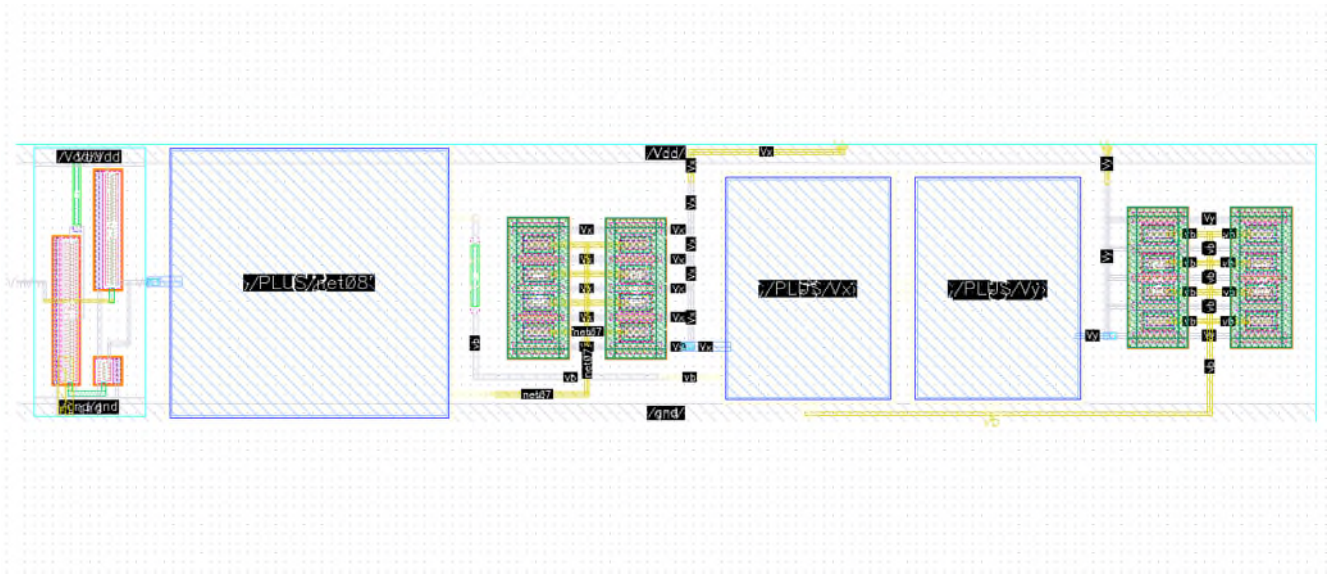

Figure 15: Source Follower together with Peak Detector Layout

Figure 16 shows the transient response of the peak detector for 50us at 500 MHz. It shows four subgraphs, one is differential output (vdiff=Vx-Vy) of the peak detector, and the other three are Vx, Vy, and input Vin of the peak detector. The red curve shows the schematic simulation results, whereas the yellow curve shows the post-layout simulation results.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

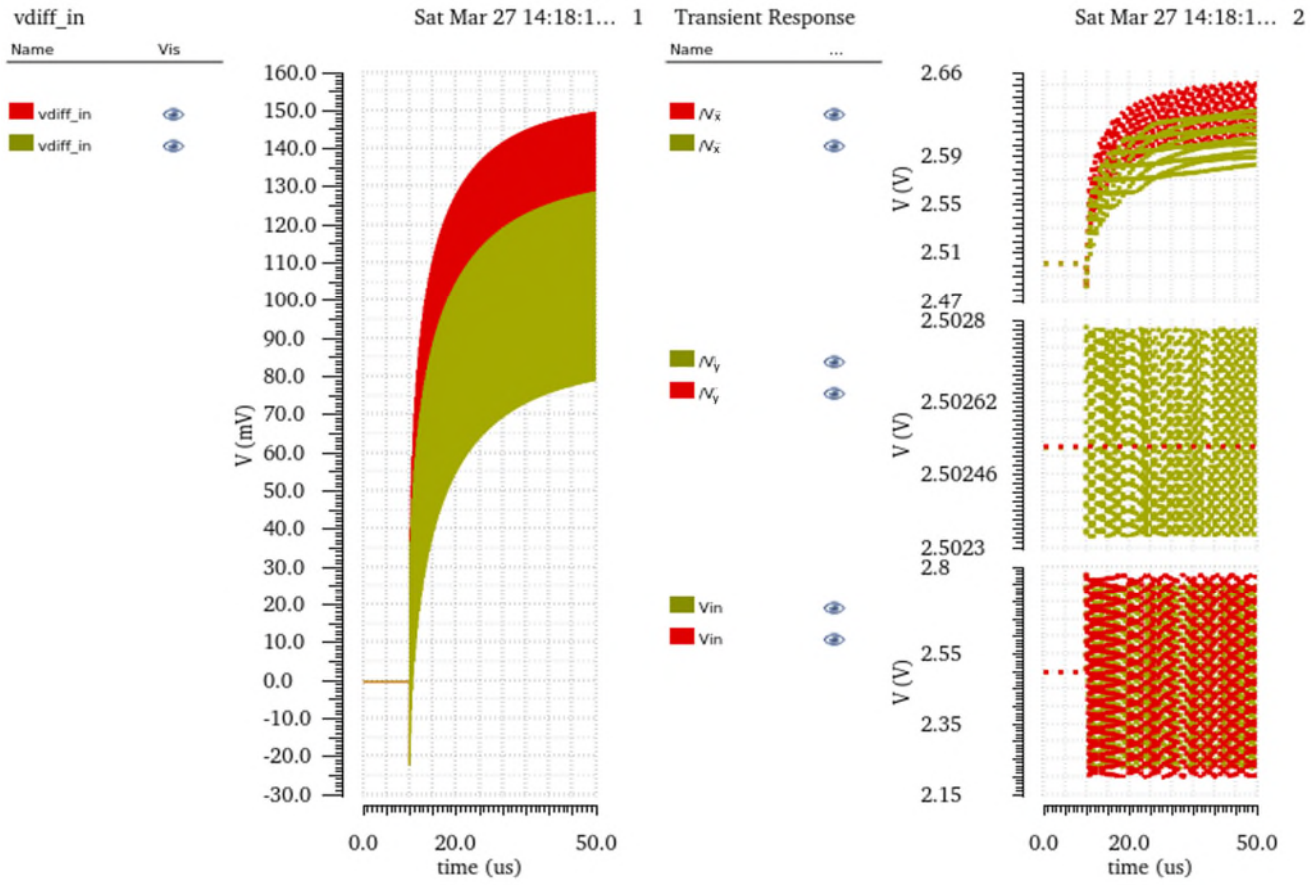

Figure 16: Transient response of Schematic (red) and Layout (yellow), Vin=277mV, Freq=500 MHz, vdiff (Vx-Vy) is differential output at Peak Detector

1.5 Analog CMOS Switch

Analog CMOS switch is a simple switch made of two transistors (NMOS and PMOS), which provides excellent switching. It can conduct analogue or digital signals in both directions when it is on and isolates the input and output of the switch when it is off.

Figure 17 shows the analogue CMOS switch with NMOS M6 and PMOS M8 transistors. The switch is on when the gate voltage of the M6 transistor is positive (5V) and the gate voltage of the M8 transistor is negative (≈0V). The switch is off when it is vice versa. Figure 18 shows the layout of the analogue CMOS switch.

The test bench for the DC response of the switch is shown in Figure 19. And the DC response of the switch is shown in Figure 20, Vin is swept from -2.5V to 2.5V for which both output voltage and output current response is observed and results were as expected.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

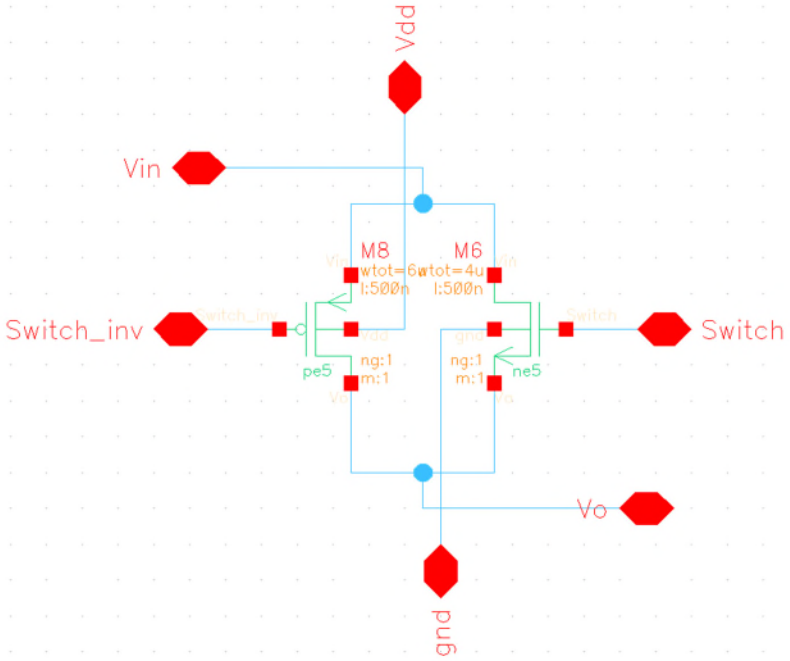

Figure 17: Analog CMOS Switch Schematic

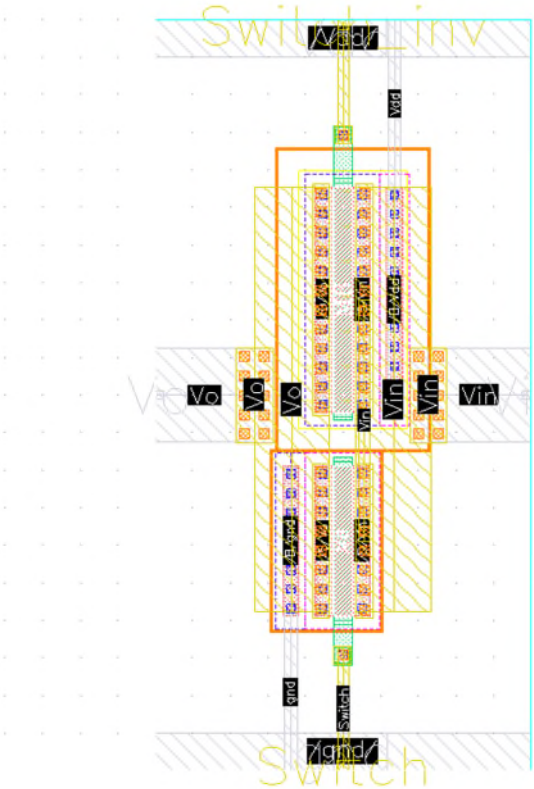

Figure 18: Analog CMOS Switch Layout

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

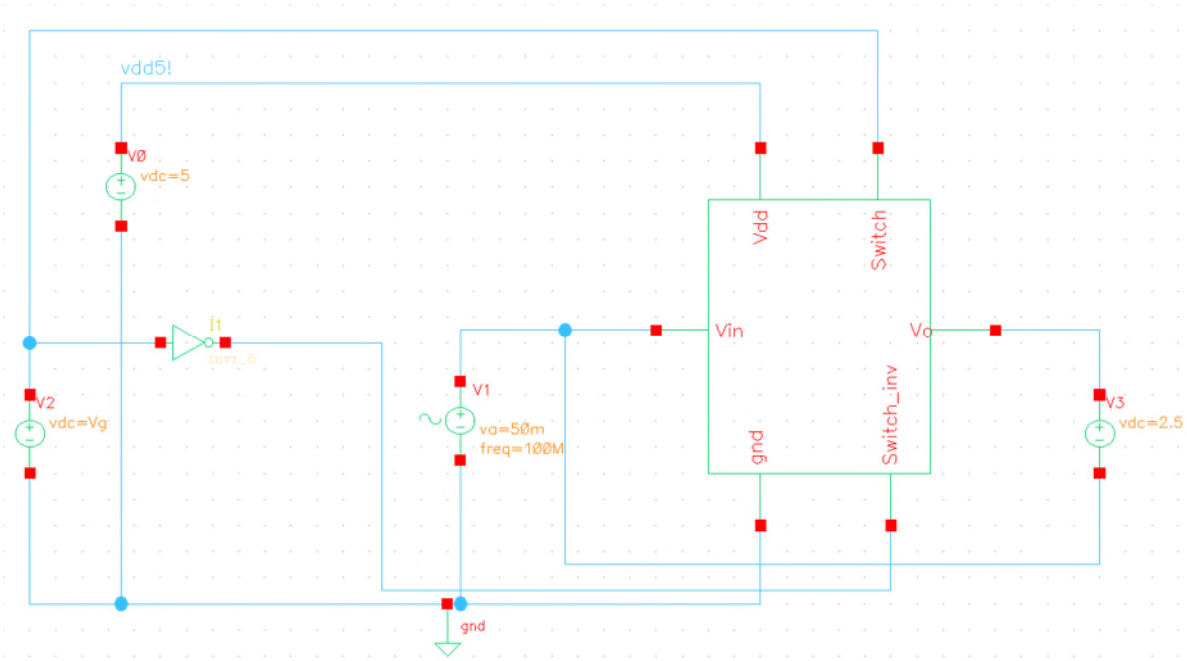

Figure 19: Test Bench for DC response of the Analog CMOS Switch

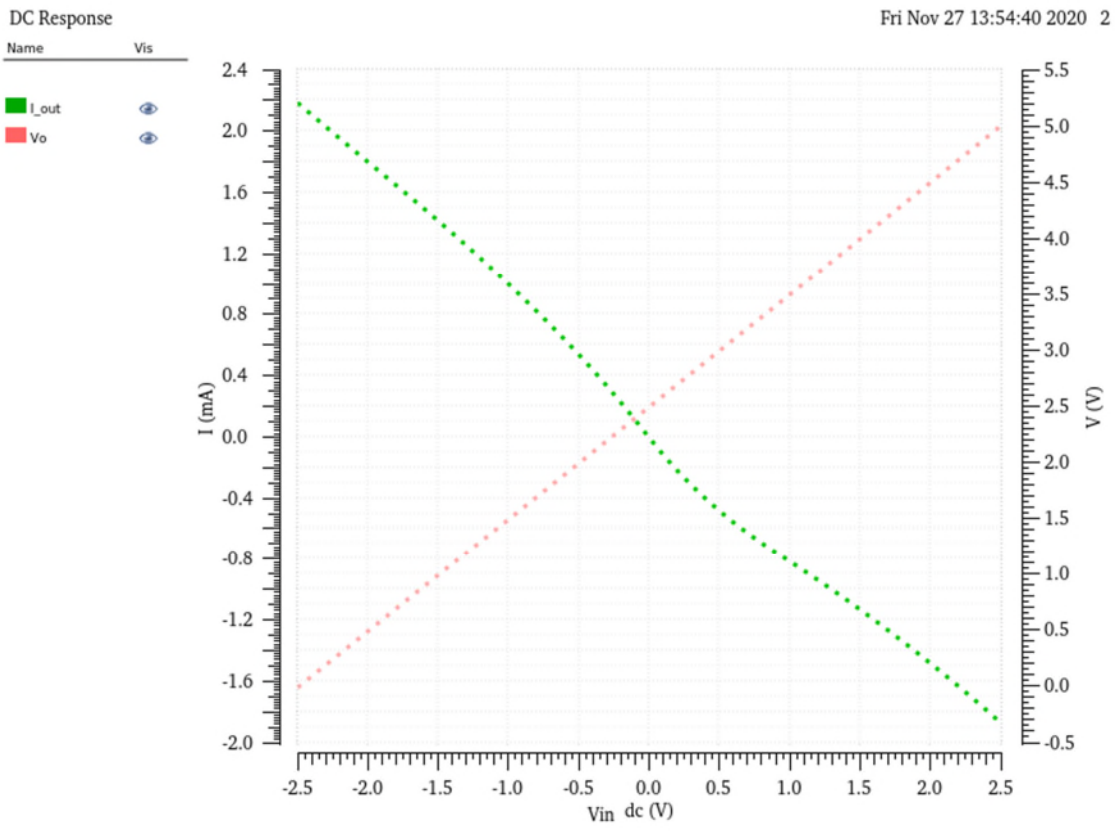

Figure 20: DC response, Input Voltage (Vin) Versus Output Voltage (Vo) and Output Current (I_out)

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

1.6 OPAMP

This Op Amp is designed using the most popular approach, the two-stage circuit architecture technique from [12]. It is unbuffered, and can provide high gain with high output swing.

Figure 21 illustrates the two-stage CMOS Op Amp with an n-channel input pair of MOSFET M1 and M2 which is differential amplifier stage. A current source (M3 and M4) is used as an active load, which allows us to achieve higher gain. MOSFET M6 is the common-source second stage A compensation capacitor is required between the Cc terminal and the output to ensure stability. The circuit is biased using and external resistor to control Ib and the current mirror transistors M5, M8 and M7.

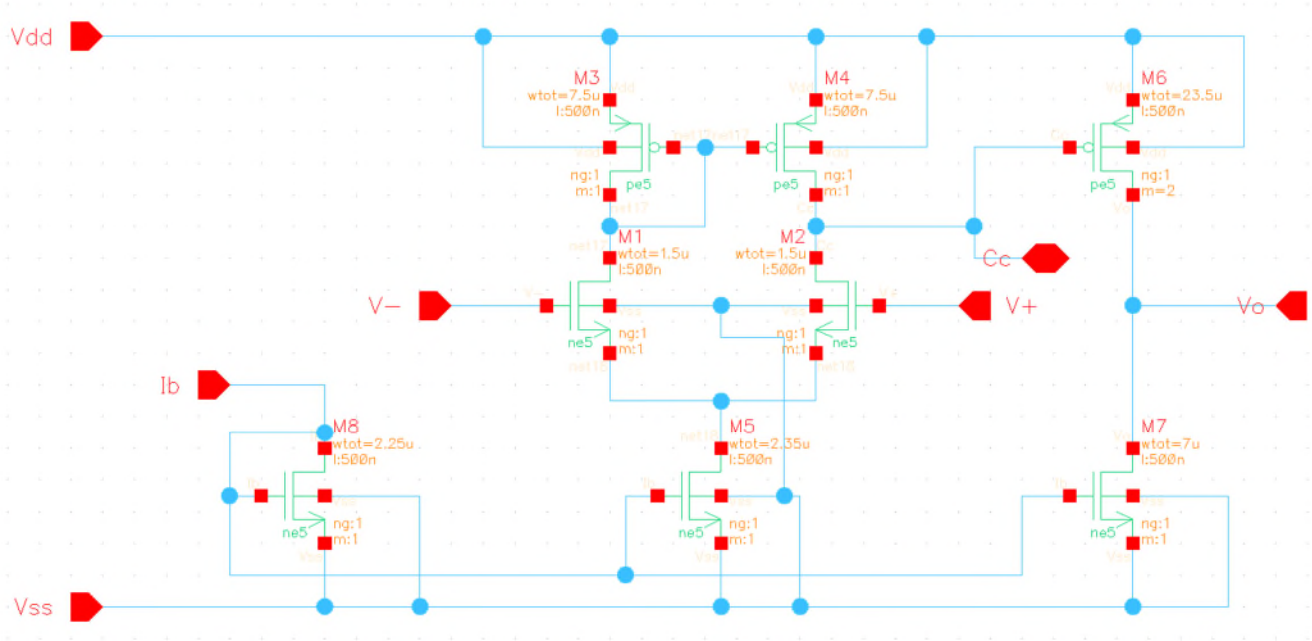

Figure 21: Schematic of an two-stage CMOS Op Amp

The test bench for open loop test is shown in Figure 23. Typically a very good stable control system has an open loop phase shift between -115^0 and -125^0, from Figure 24 the open loop phase shift of our Op Amp is -117.72^0. As shown in Figure 25, the input offset voltage is around 400 µV which is due to current mirror error of the active load M3 and M4.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

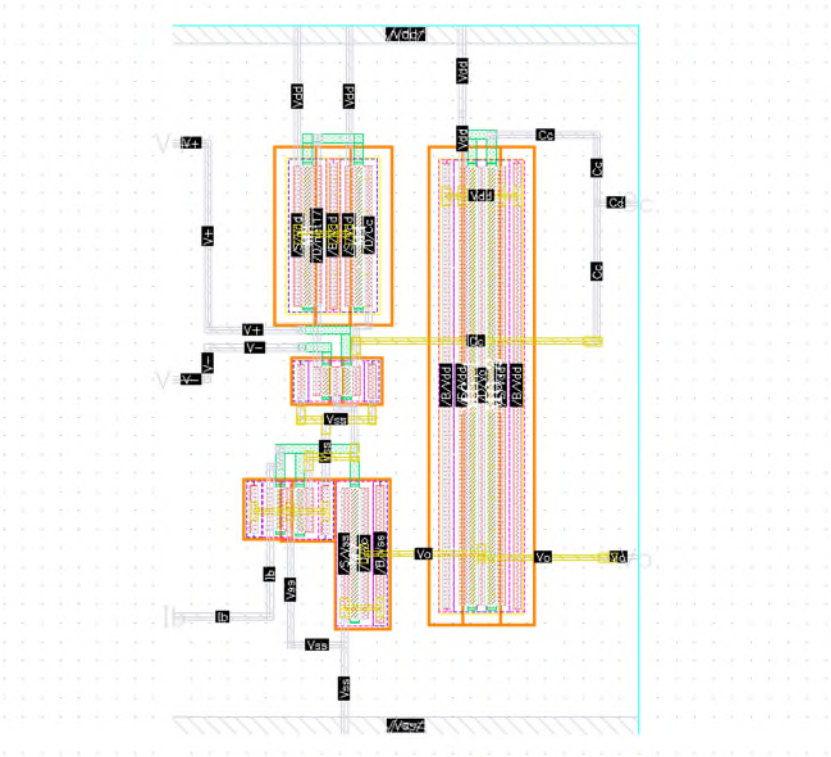

Figure 22: Layout of an two-stage CMOS Op Amp

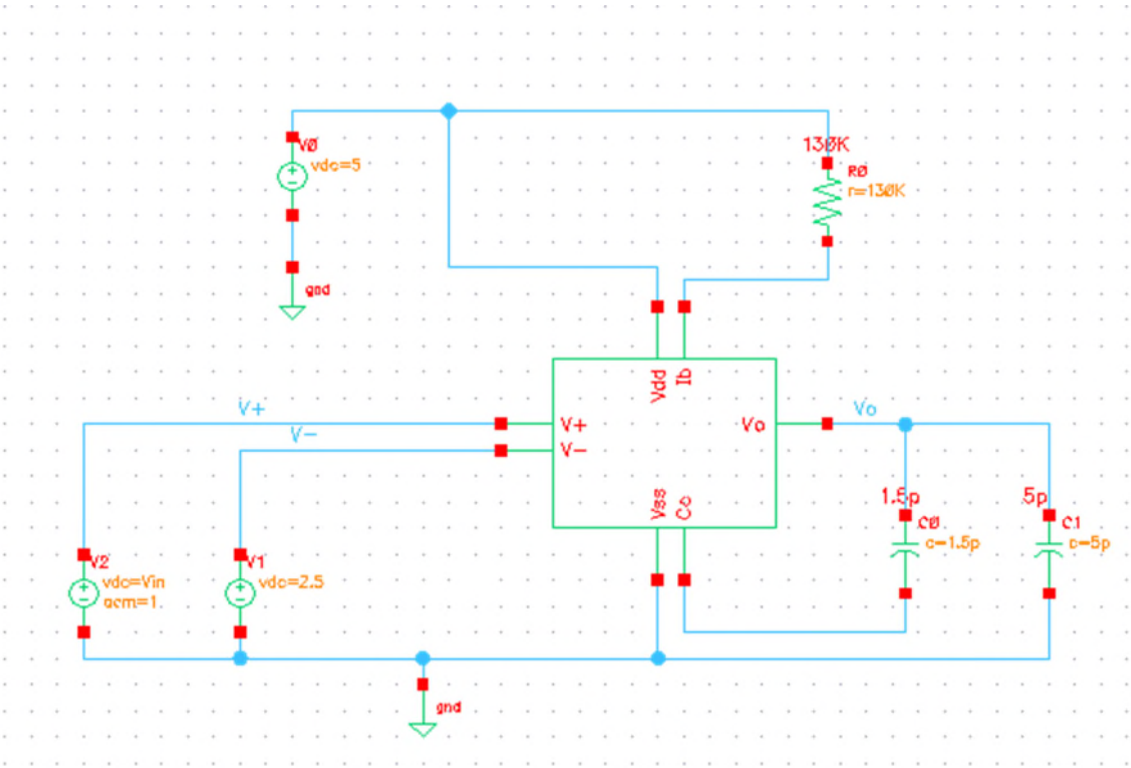

Figure 23: Test Bench for Open Loop Tests

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

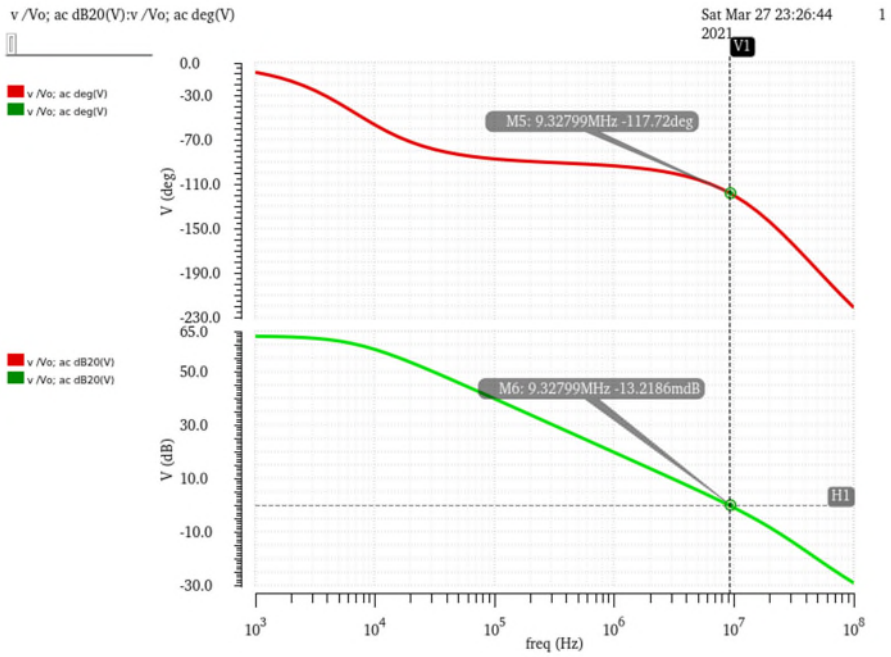

Figure 24: AC magnitude (bottom) and Phase (top) of schematic (Red) and post-layout simulation (Green), Phase Margin =-117.72-(-180)=62.28, Gain Bandwidth =9.32 MHz

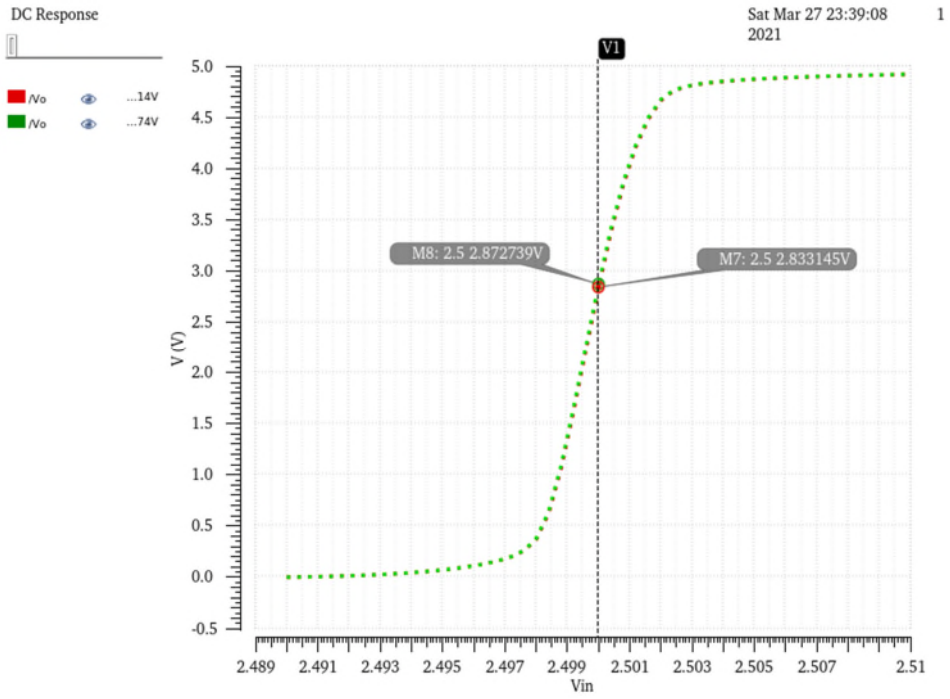

Figure 25: DC response of schematic (red) and post-layout simulation (green), Input offset voltage is 400 µV

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

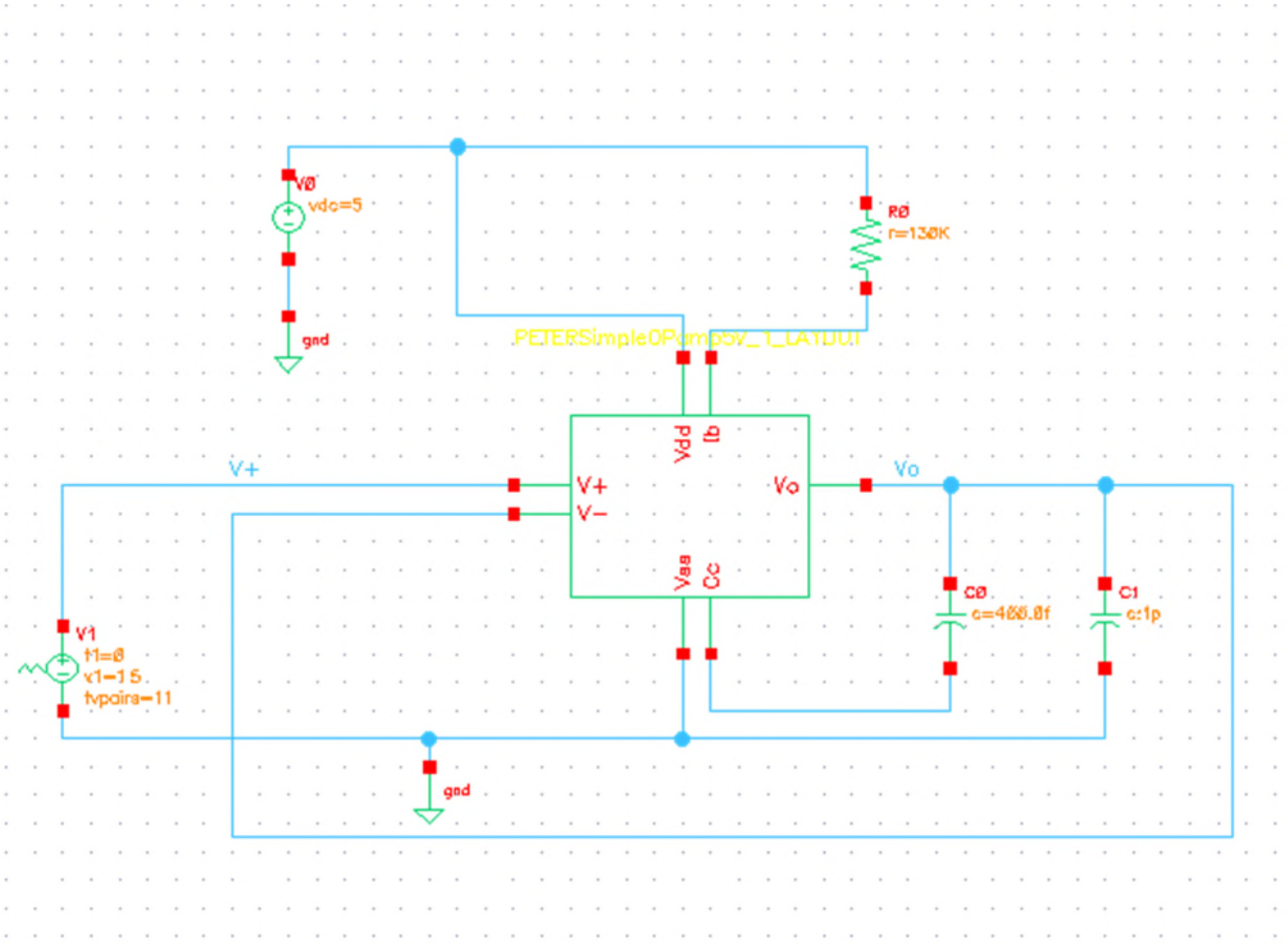

Figure 26: Test Bench for Unity Gain Tests

Test bench for unity gain tests is shown in Figure 26. Bias current (Ib) is given externally, a compensation capacitor (C0) is connected between the pin Cc and Vo. Figure 27 shows the input common mode range (ICMR) which is from 1.5V to 5V. Figure 28, Figure 29, and Figure 30 shows frequency response of output voltage, frequency response of the current which is flowing through the transistor M5, and transient response of the Op Amp respectively.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

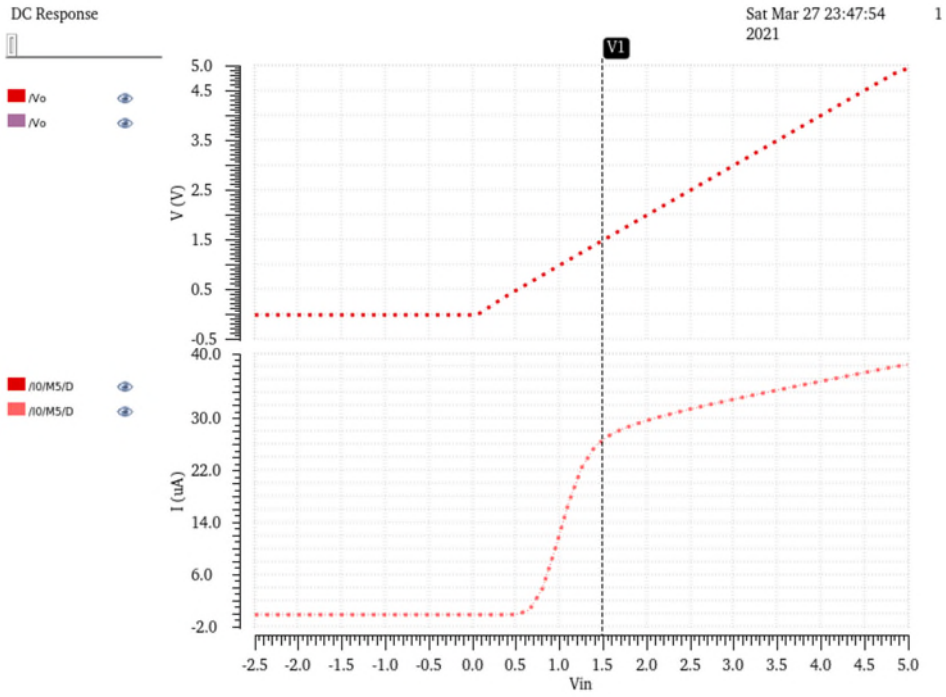

Figure 27: Input Common Mode Range (ICMR), is from 1.5V to 5V. Figure shows both schematic (red) and post-layout (pink) simulation

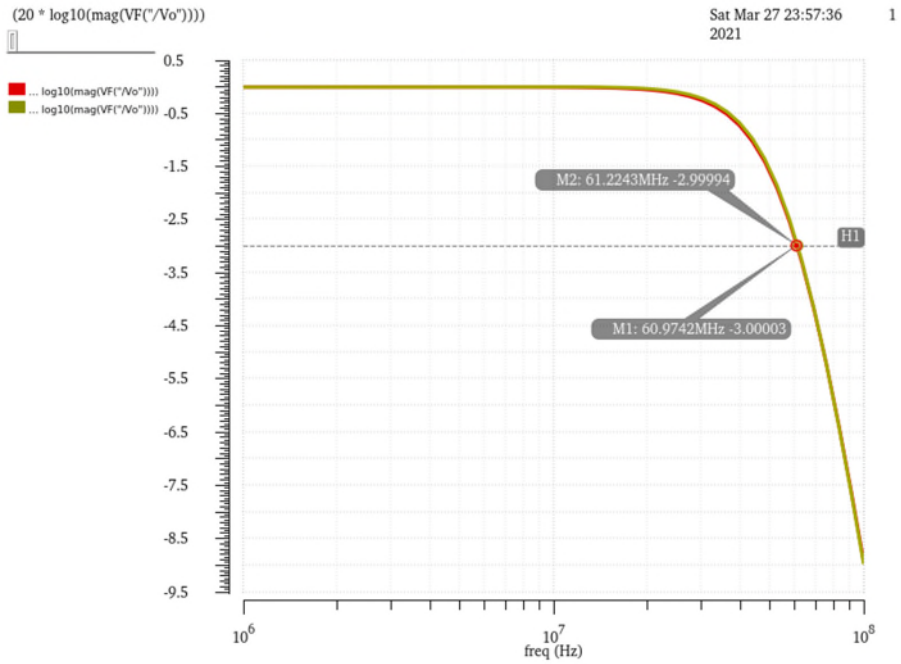

Figure 28: Frequency Response of output voltage in dB and gain is unity. Figure shows both schematic (red) and post-layout (yellow) simulation

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

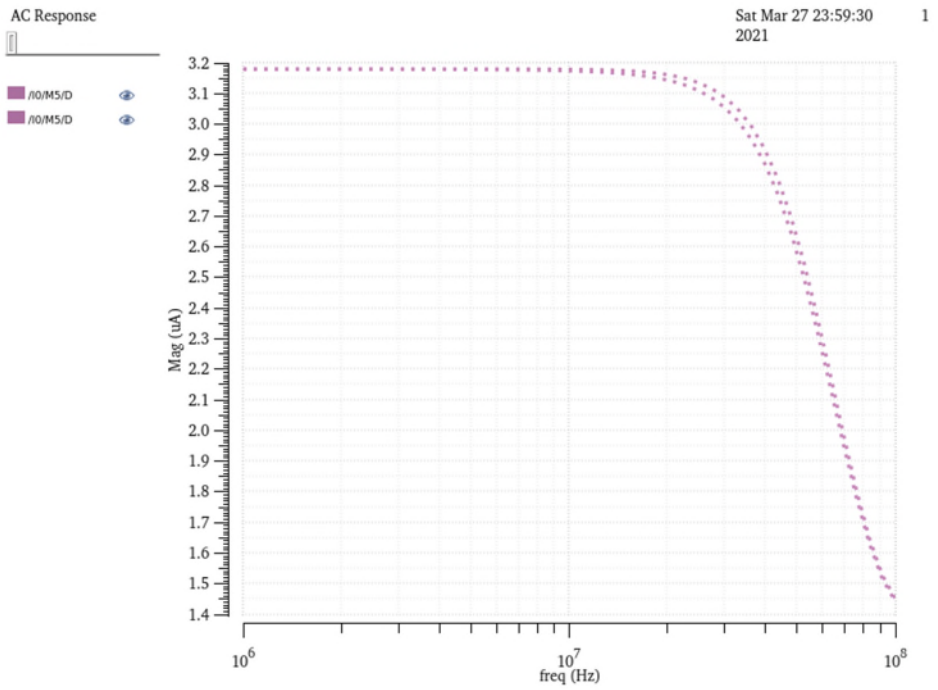

Figure 29: Frequency Response, AC current through M5 transistor, Figure shows both schematic (red) and post-layout (pink) simulation

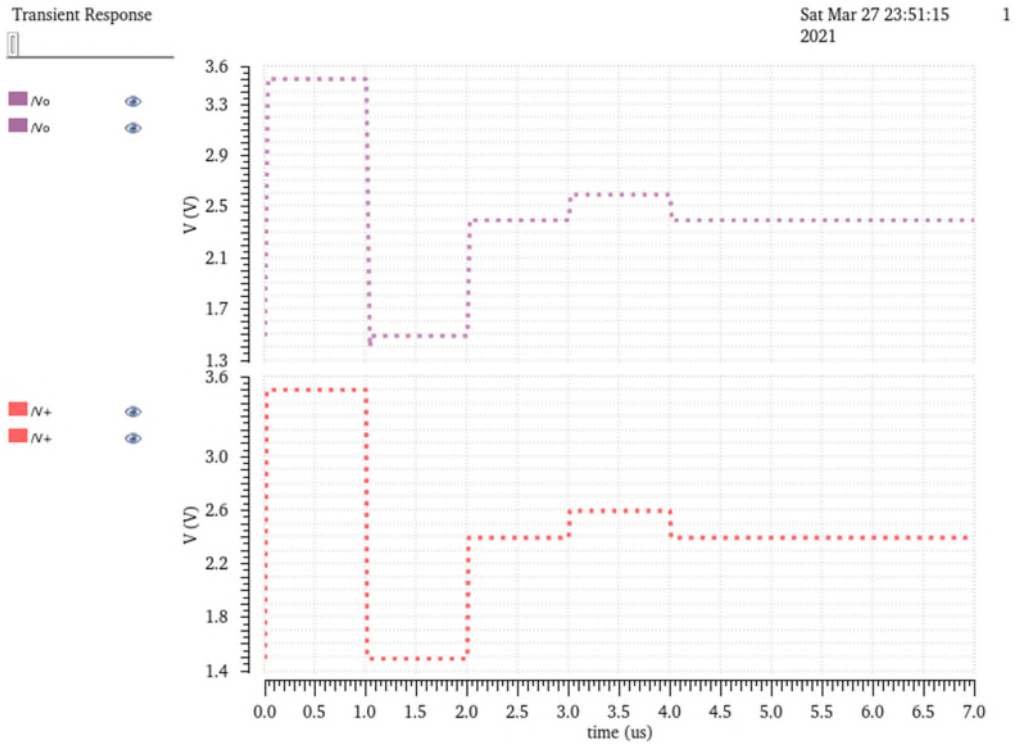

Figure 30: Transient Response of output voltage (Vo) and input voltage (V+), schematic and post-layout simulation

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

1.7 Instrumentation Amplifier

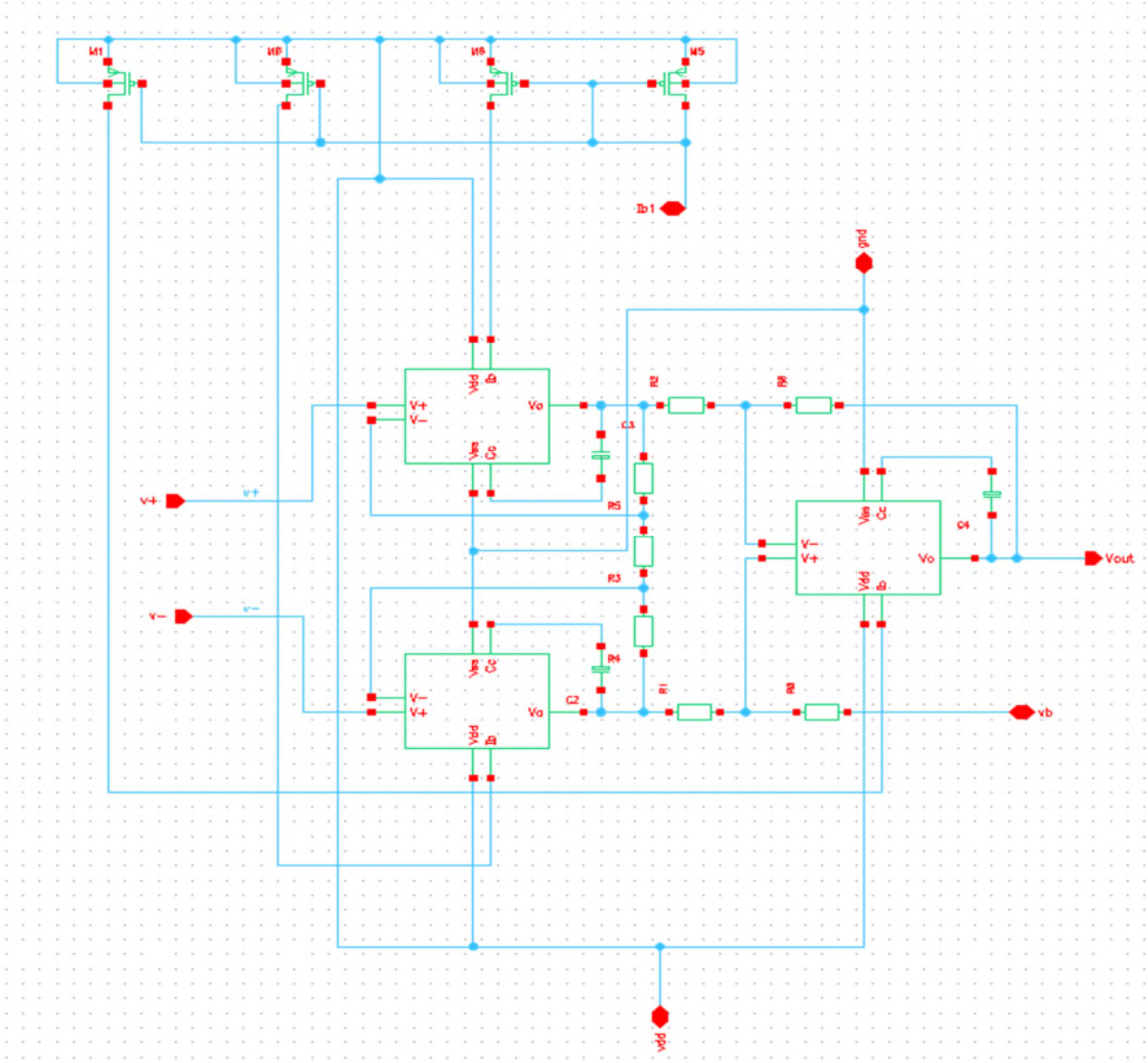

Figure 31: Instrumentation Amplifier Schematic

The Instrumentation Amplifier (IA) shown in Figure 31 is built using the Op Amp designed in previous section. It incorporates three Op Amps, two of them behave as input buffer amplifiers and the third Op Amp behaves as a differential amplifier. External bias current for Op Amps are mirrored using current mirror configuration using M1, M0, M8 and M5 transistors. The gain of the IA is controlled by the resistors used in between the Op Amps.

The layout and test bench of the instrumentational amplifier is as shown Figure 32 and Figure 33 respectively. Both schematic and post-layout simulations is very close enough.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

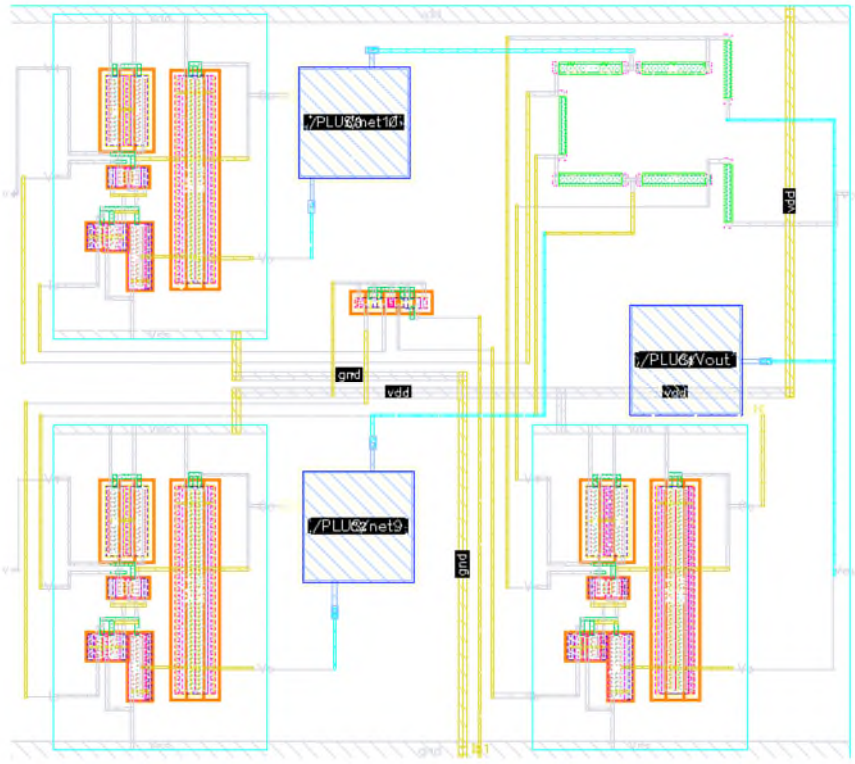

Figure 32: Instrumentation Amplifier Layout

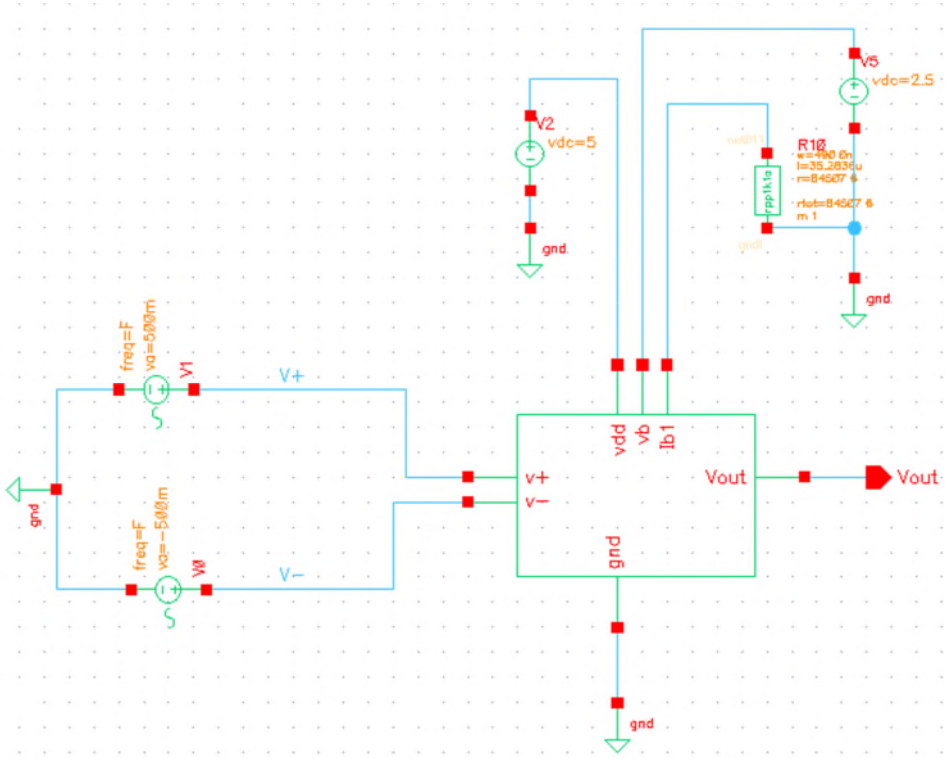

Figure 33: Test bench for Instrumentation Amplifier

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

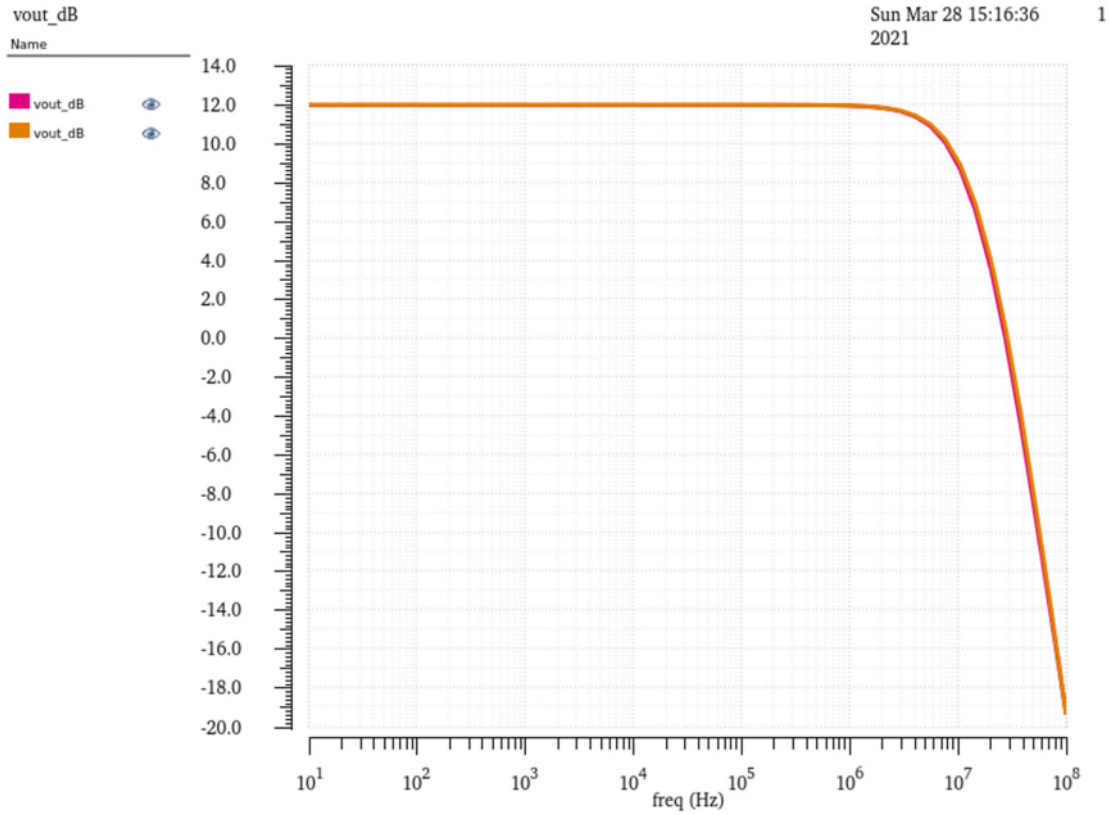

Figure 34: Frequency Response of the Instrumentation Amplifier, which has a gain of 4 (12dB), compares both schematic (pink) and post-layout (yellow) simulation.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

1.8 3 to 8 Line Decoder

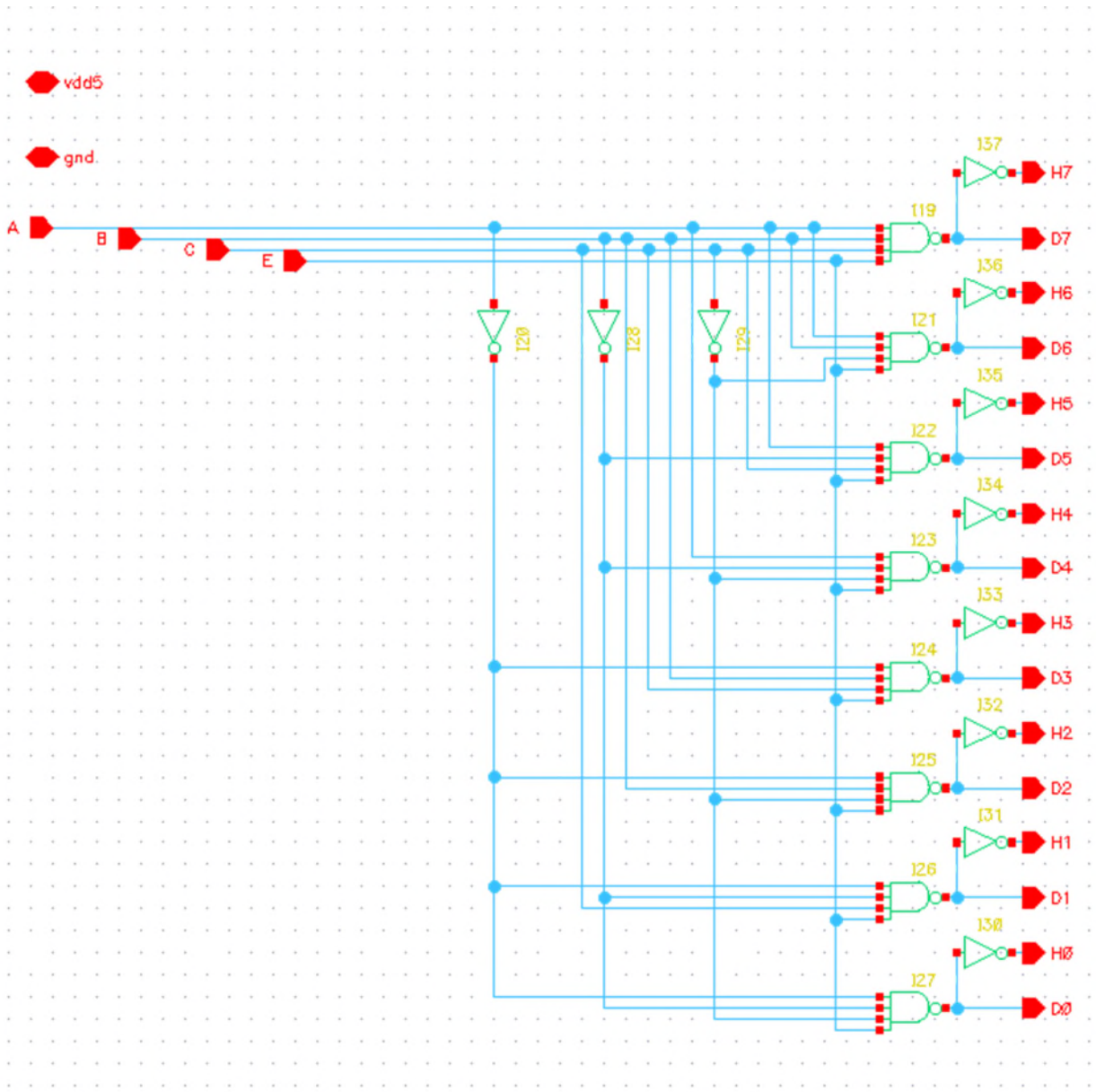

Figure 35: 3 to 8 Line Decoder Schematic

A 3 to 8-line decoder is also called a 3 to 8-line selector. It is designed using eight four-input NAND gates as shown in Figure 35. To get both high and low outputs, eight inverters are also used at the output of the decoder. As the name suggests the decoder has three inputs A, B, C, and an Enable (E) with eight outputs D0 to D7 & H0 to H7.

This decoder activates one output in D0 to D7 for every 3 bits binary input value from 0 to 7. The layout of the 3 to 8 line decoder is as shown in Figure 36. Schematic and post-layout simulation of input and outputs are shown in Figure 37, Figure 38, and Figure 39. There is no

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

visual difference between schematic and post-layout simulation since we are dealing with block-level simulations.

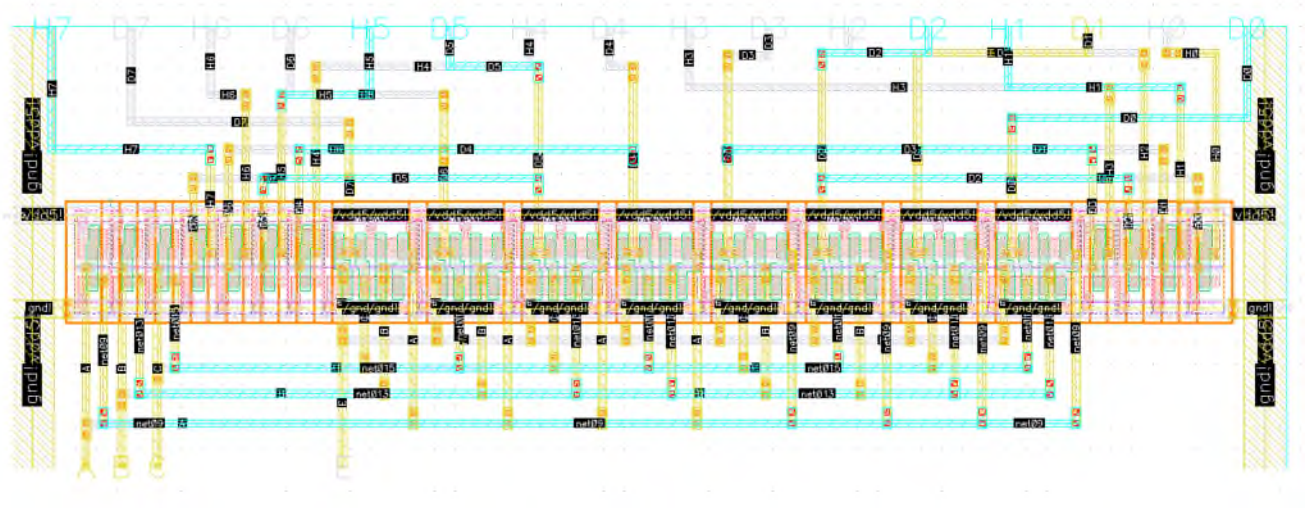

Figure 36: 3 to 8 Line Decoder Layout

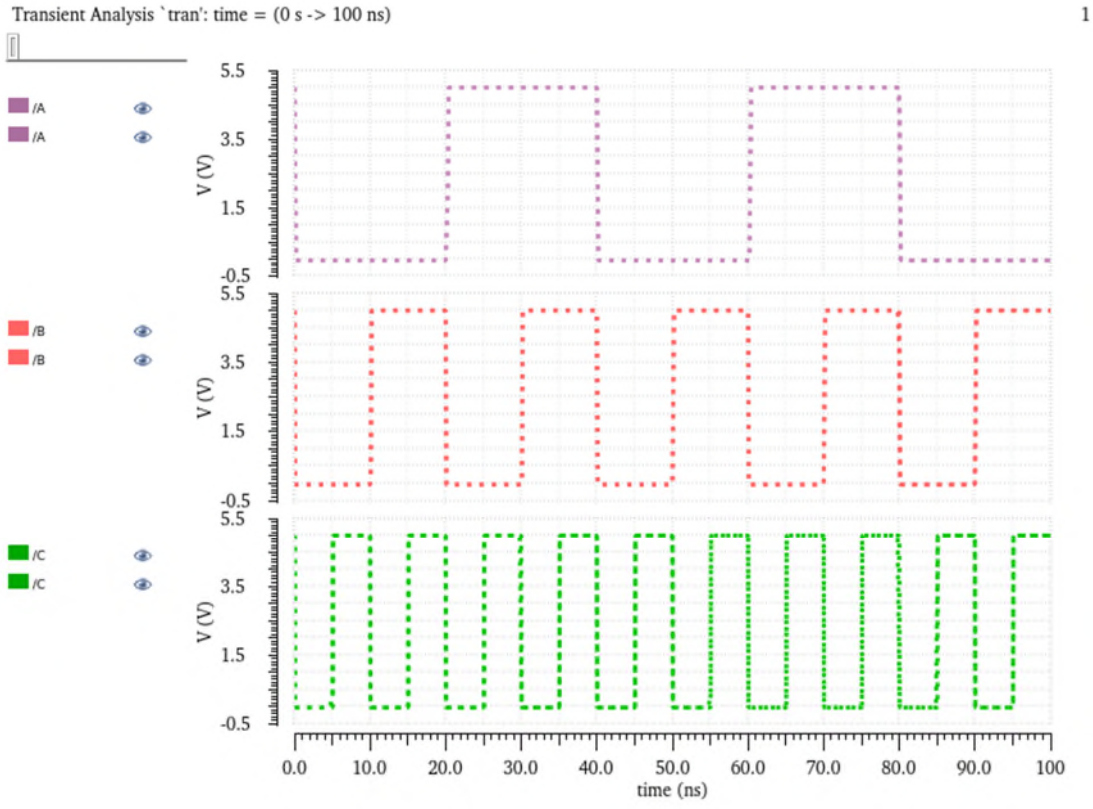

Figure 37: Input of 3 to 8 Line Decoder

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

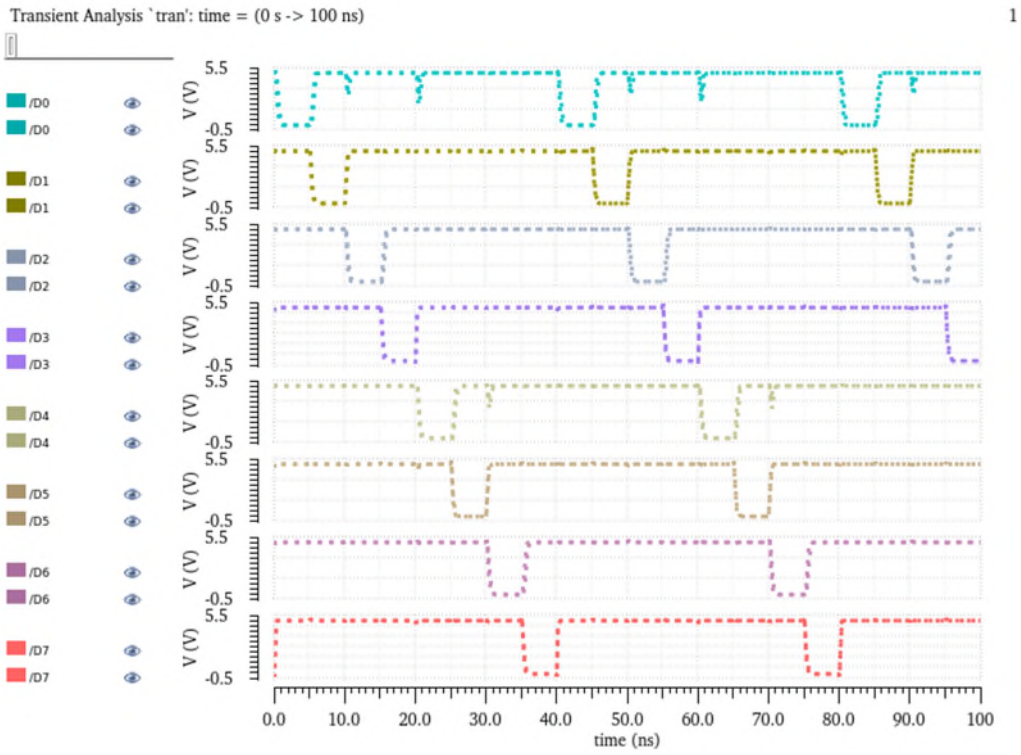

Figure 38: Output of 3 to 8 Line Decoder, active low

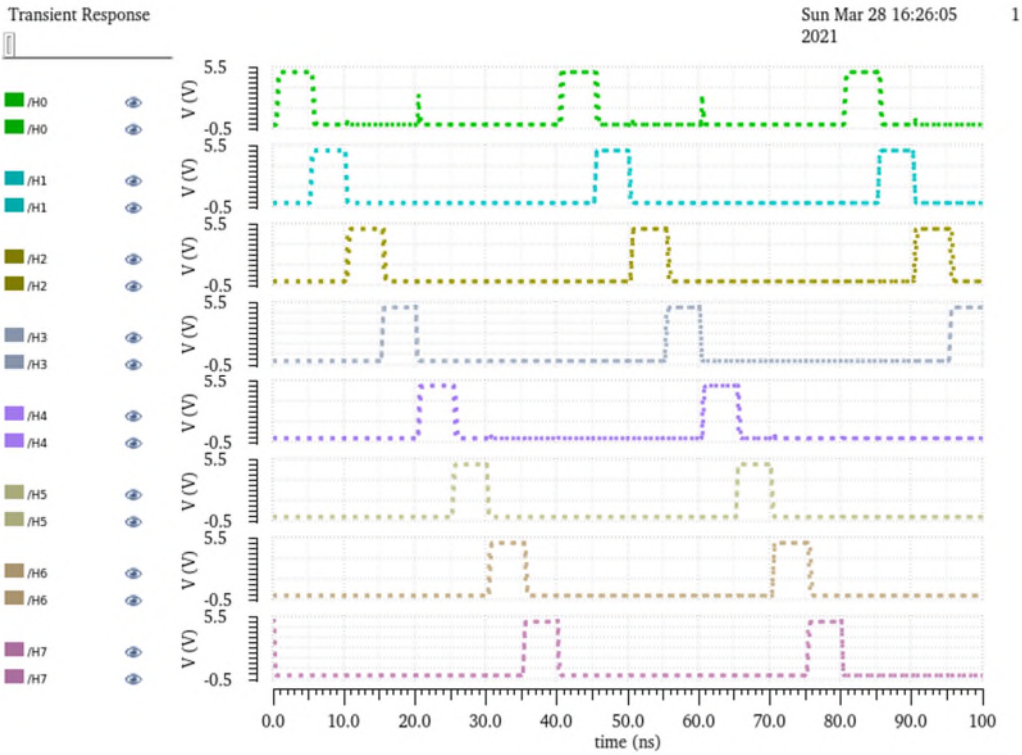

Figure 39: Output of 3 to 8 Line Decoder, active high

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

3. Channel 0 to 7 Circuit, Layout and Simulation Results

1.9 Channel 0 or 4

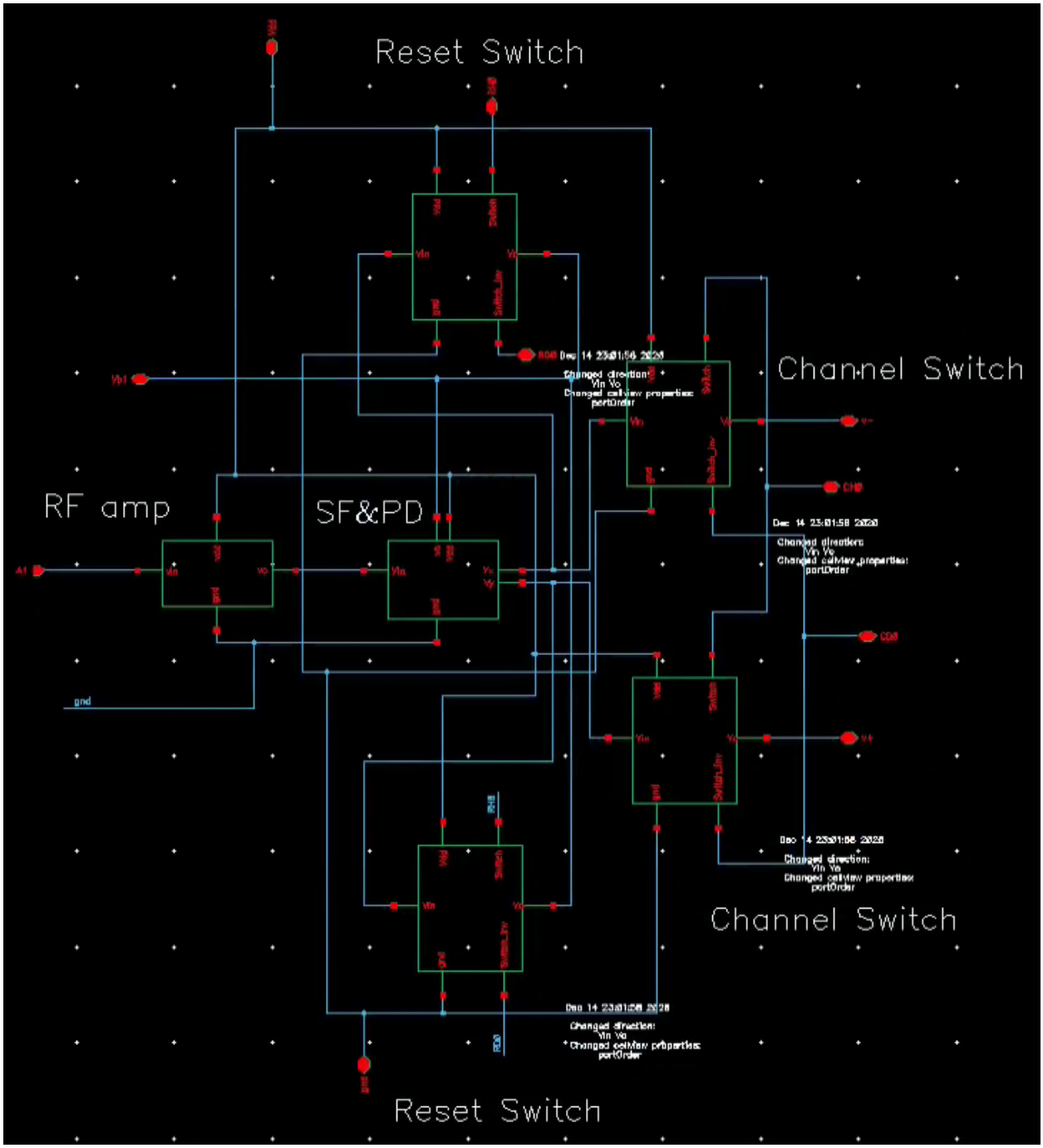

Figure 40: Channel 0 or 4 Schematic

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

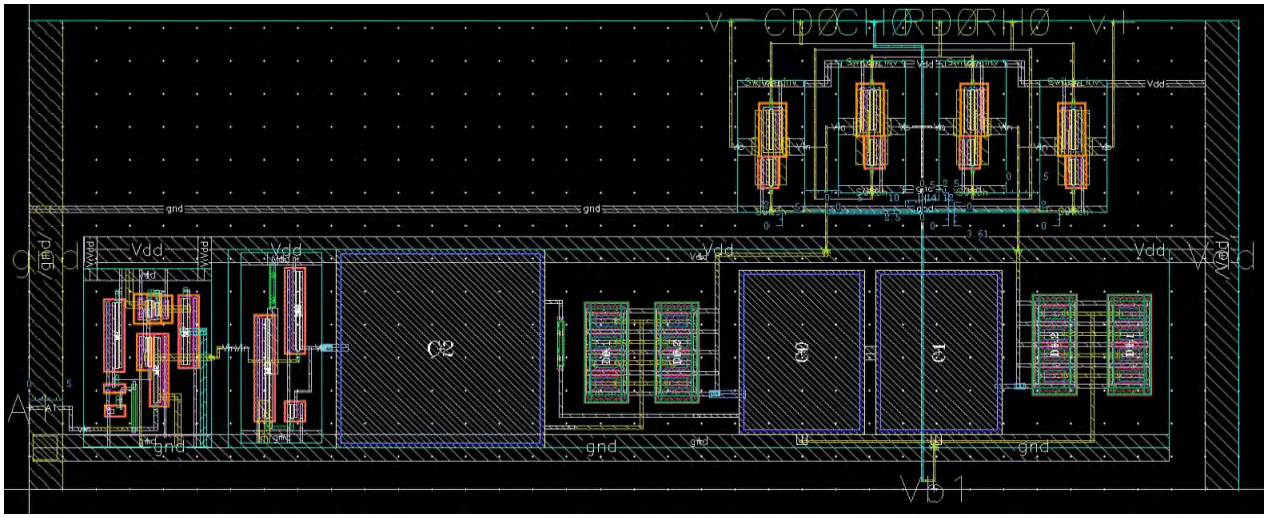

Figure 41: Channel 0 or 4 layout

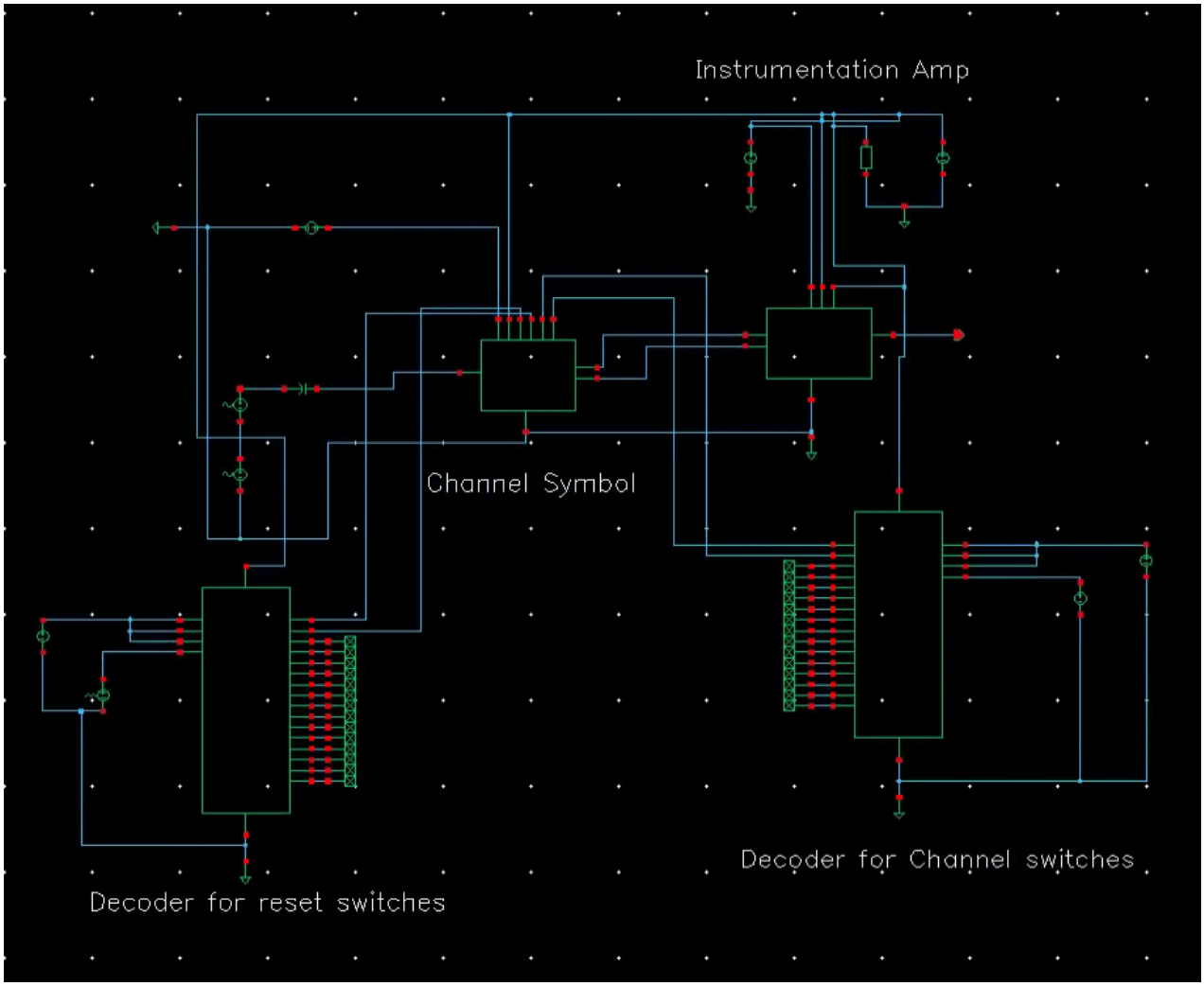

Figure 42: Test Bench for Channel block

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

The minimum voltage required for the peak detector to detect the signal is 50mV. Hence, to detect lower signals we need an amplifier before the peak detector stage. This is where our designed high gain RF amplifier and broadband RF amplifier come to the picture, which will be placed before the peak detector stage. To protect the gain-bandwidth of the RF amplifier a source follower is used between the peak detector and RF amplifier. In this chapter, we simulate all these stages together with different configurations explained in Chapter 1, Figure 2. The first configuration is channel 0 or 4 which is shown in Figure 40. All these different configurations such as channels 0 to 3 or channels 4 to 7 will be simulated using the test bench shown in Figure 42. All these different configurations have different sensitivity levels, in other words, different detection levels.

As already illustrated in Figure 2, the peak detector is connected to Instrumentation Amplifier through channel switches which can be seen in Figure 42.

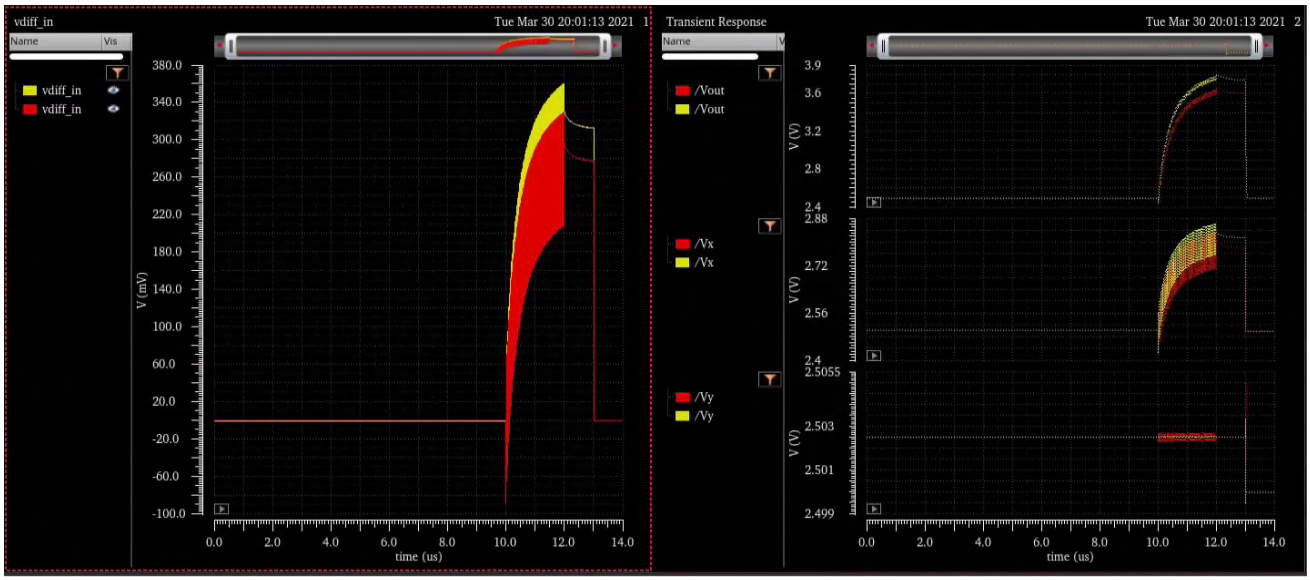

Figure 43: Transient Response of Channel 0 or 4 Schematic (yellow) and Layout (red), Vin=50mV, Freq=50 MHz, vdiff (Vx-Vy) is differential output at Peak Detector, Vout is the output at Instrumentation Amplifier

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

1.10 Channel 1 or 5

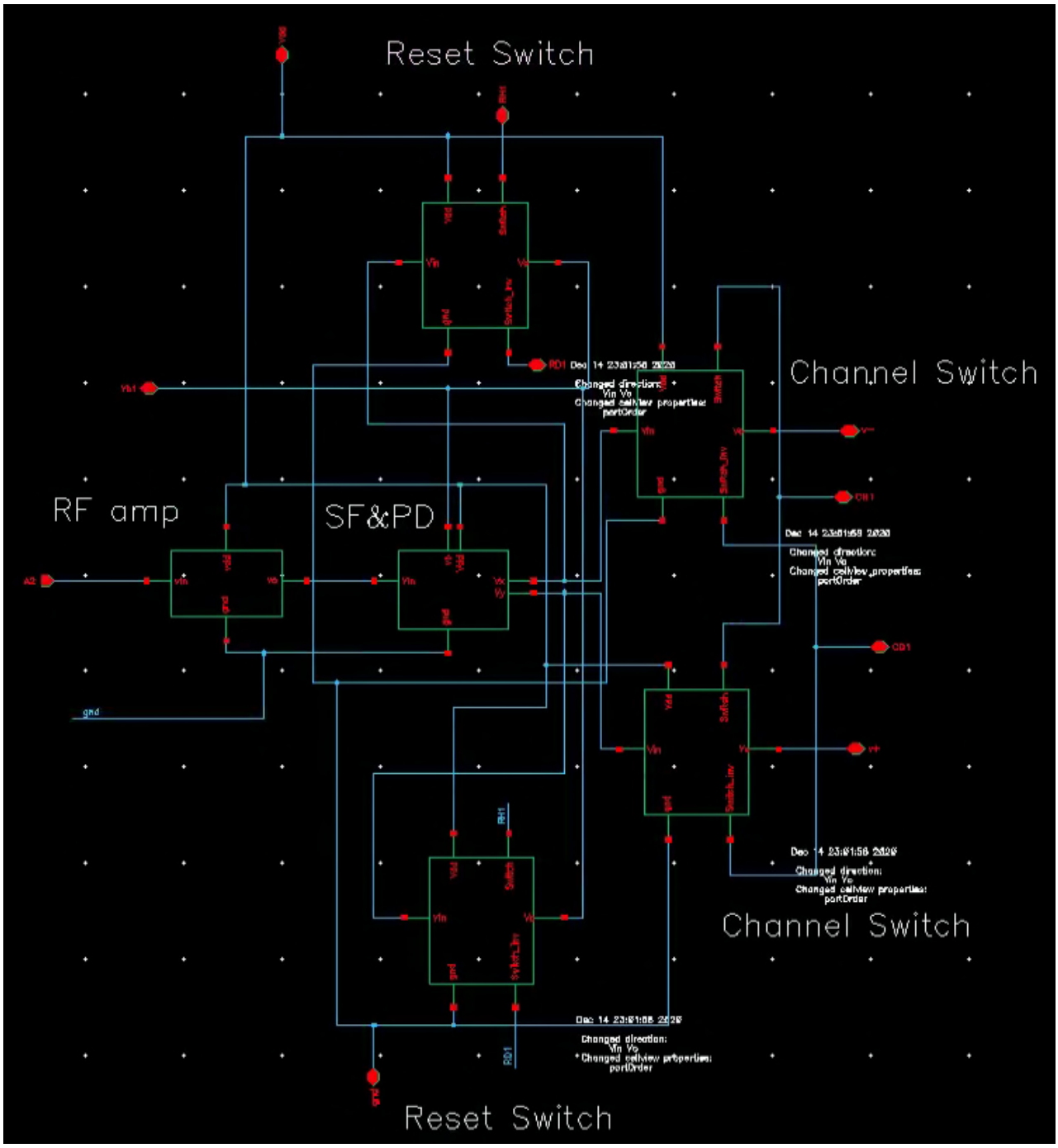

Figure 44: Channel 1 or 5 Schematic

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

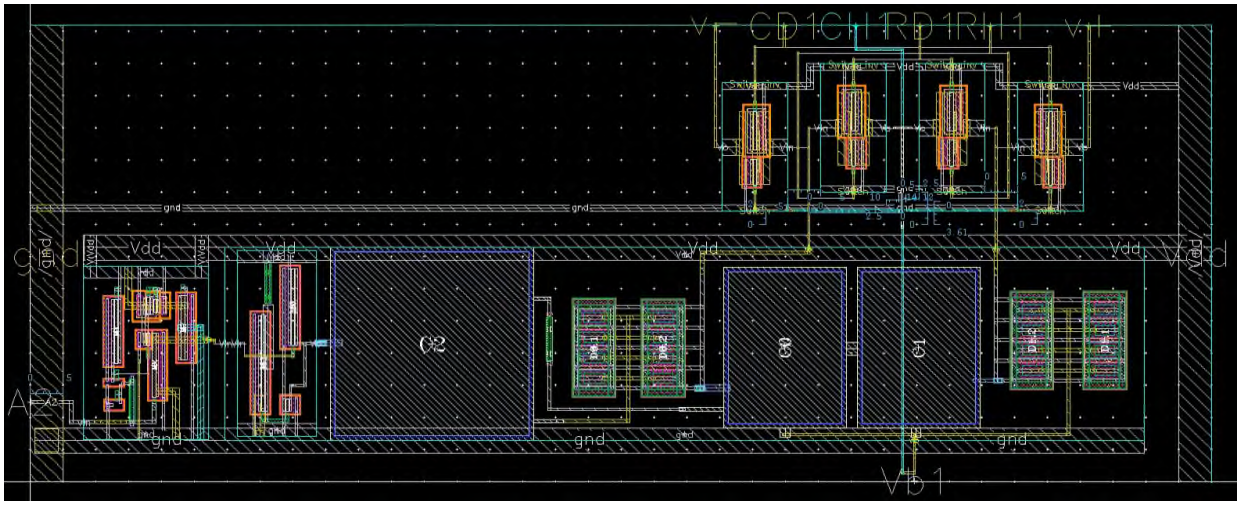

Figure 45: Channel 1 or 5 Layout

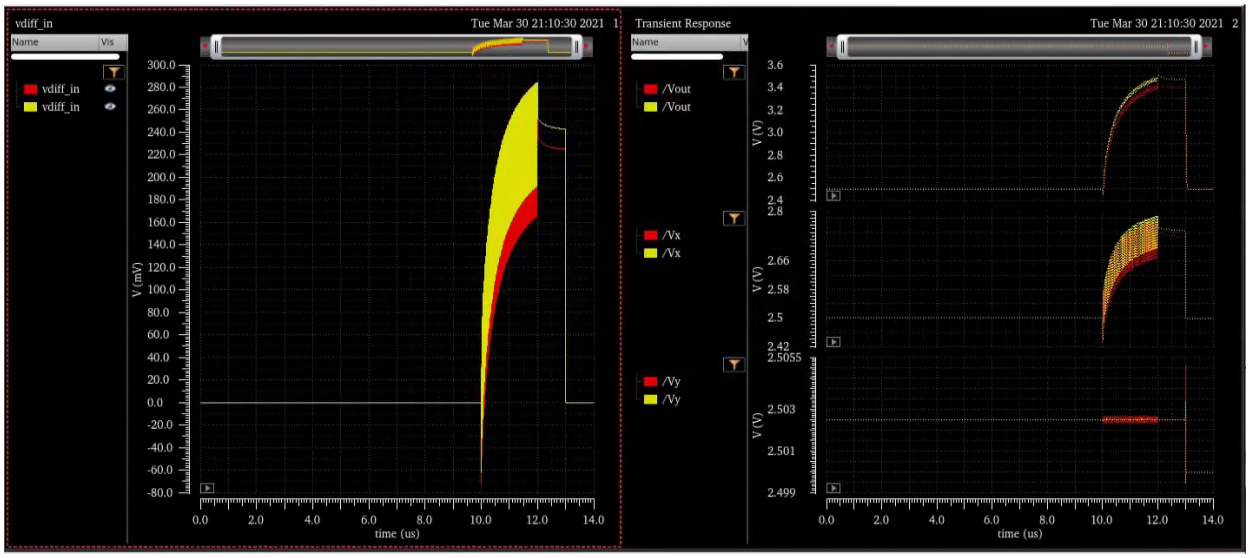

Figure 46: Transient Response of Channel 1 or 5 Schematic (yellow) and Layout (red), Vin=100mV, Freq=50 MHz, vdiff (Vx-Vy) is differential output at Peak Detector, Vout is the output at Instrumentation Amplifier

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

1.11 Channel 2 or 6

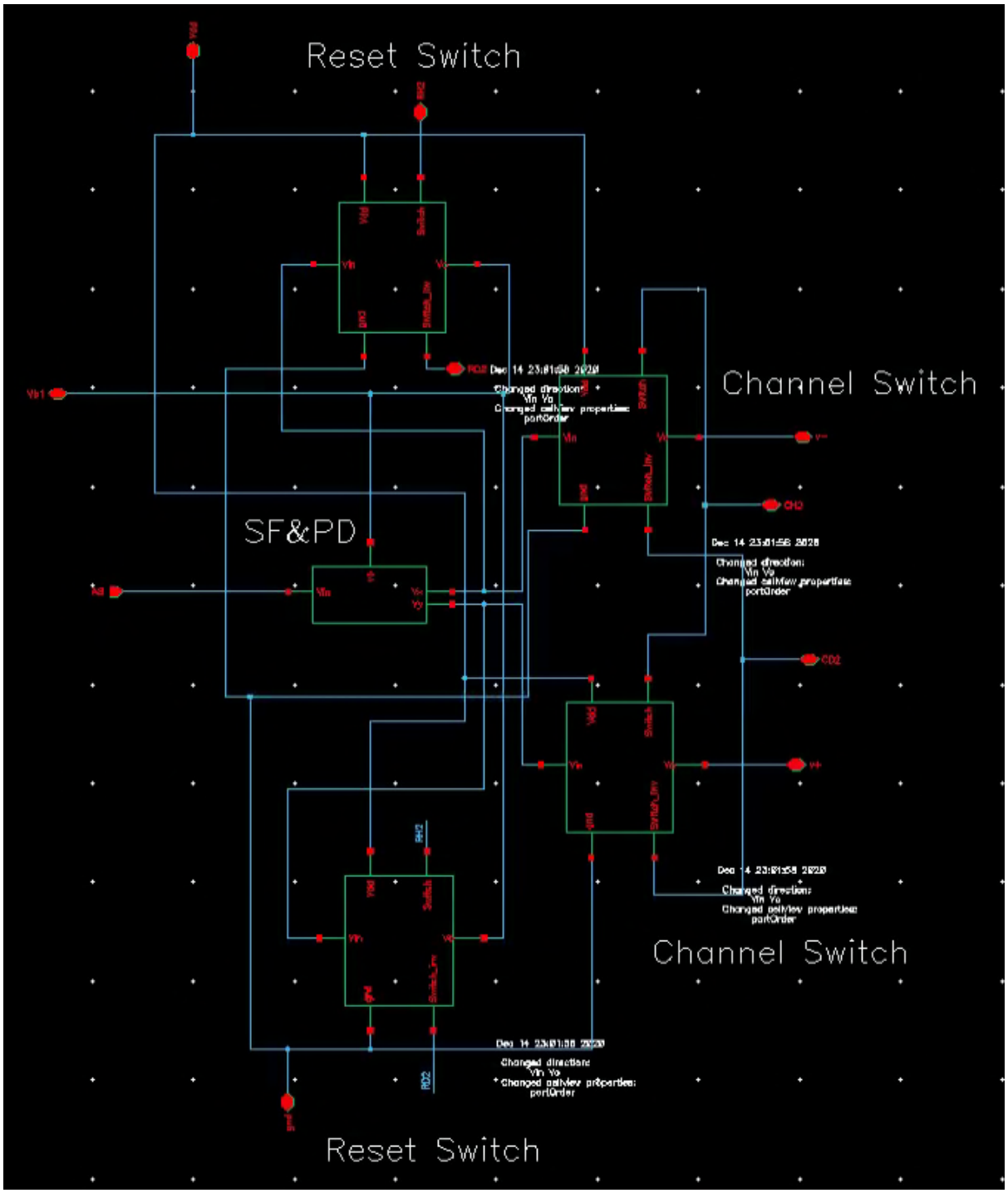

Figure 47: Channel 2 or 6 Schematic

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

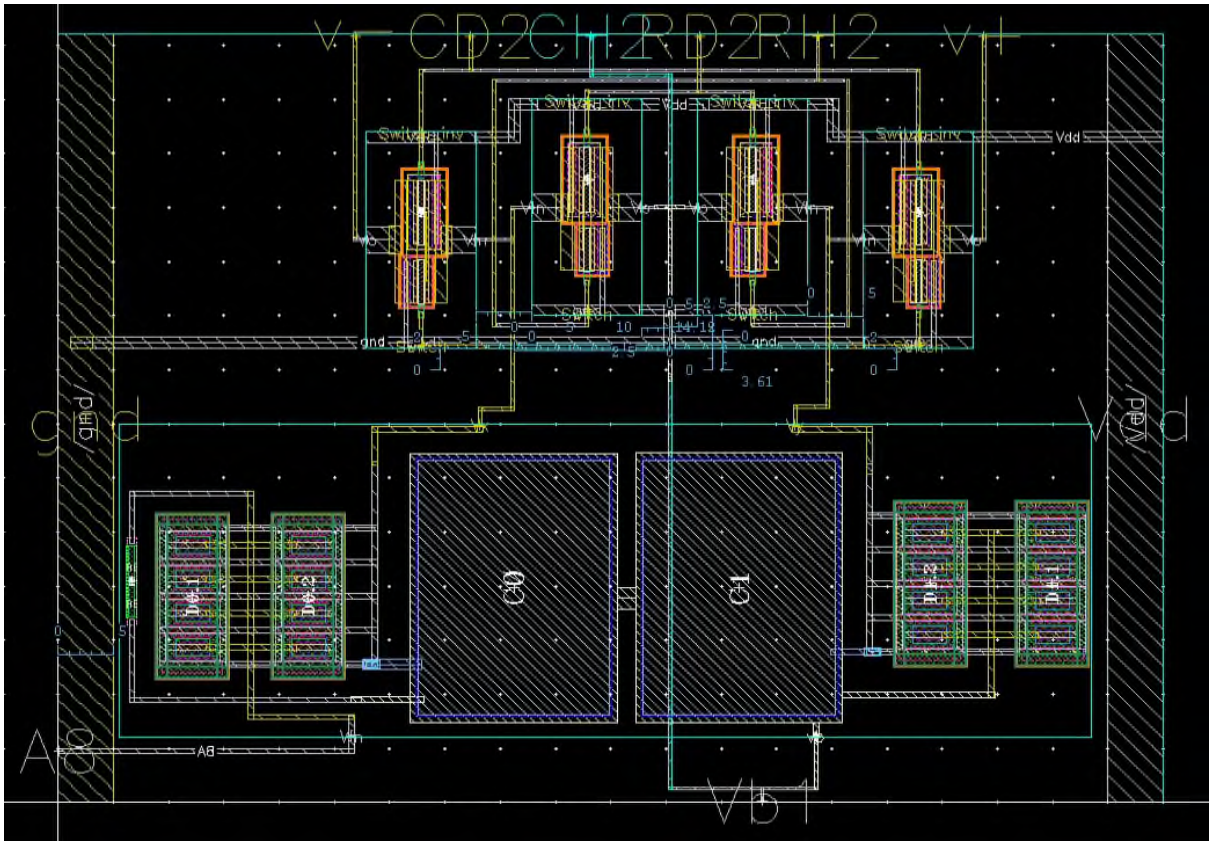

Figure 48: Channel 2 or 6 layout

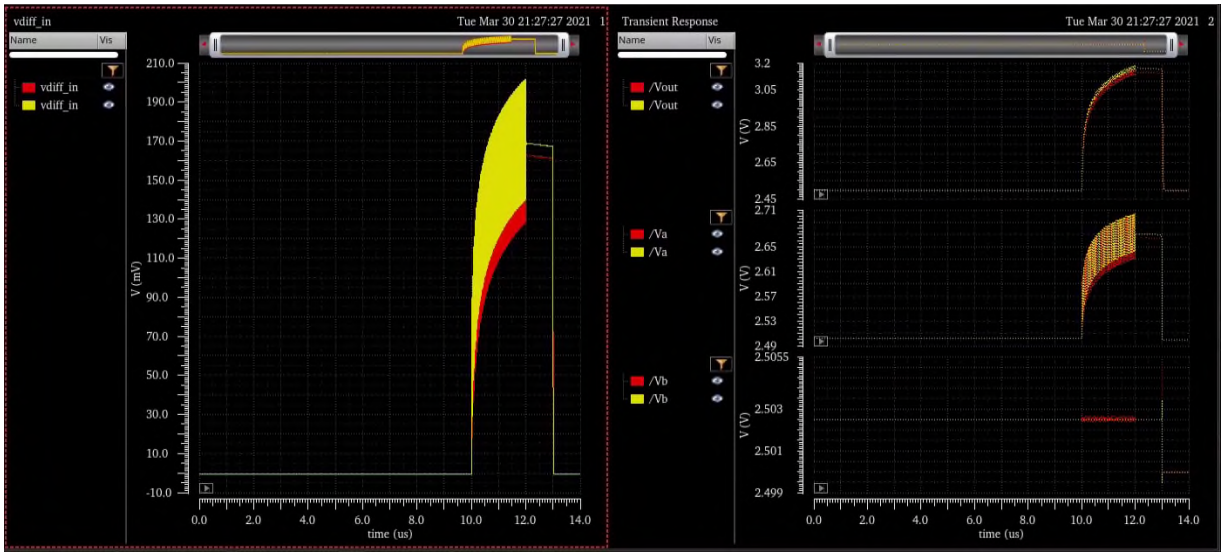

Figure 49:Transient Response of Channel 2 or 6 Schematic (yellow) and Layout (red), Vin=400mV, Freq=50 MHz, vdiff (Va-Vb) is differential output at Peak Detector, Vout is the output at Instrumentation Amplifier

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

1.12 Channel 3 or 7

Channels 3 and 7 simply connect directly to the instrumentation amplifier through the analogue switched controlled by the channel selection multiplier. This allows connection directly to the instrumentation amplifier for test purposes and allows the possibility of other external detectors or exploring the effect of ref inputs directly to the instrumentation amplifier. The channel multiplexer switch circuit is shown in Figure 50 and the layout of the switches is shown in Figure 51.

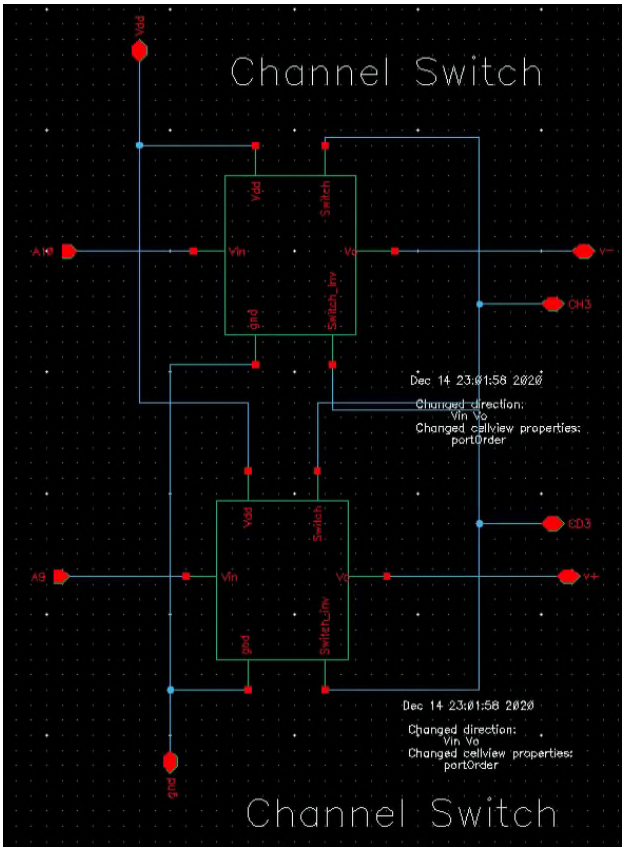

Figure 50: Channel 3 or 7 Schematic, it has only two-channel switches

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

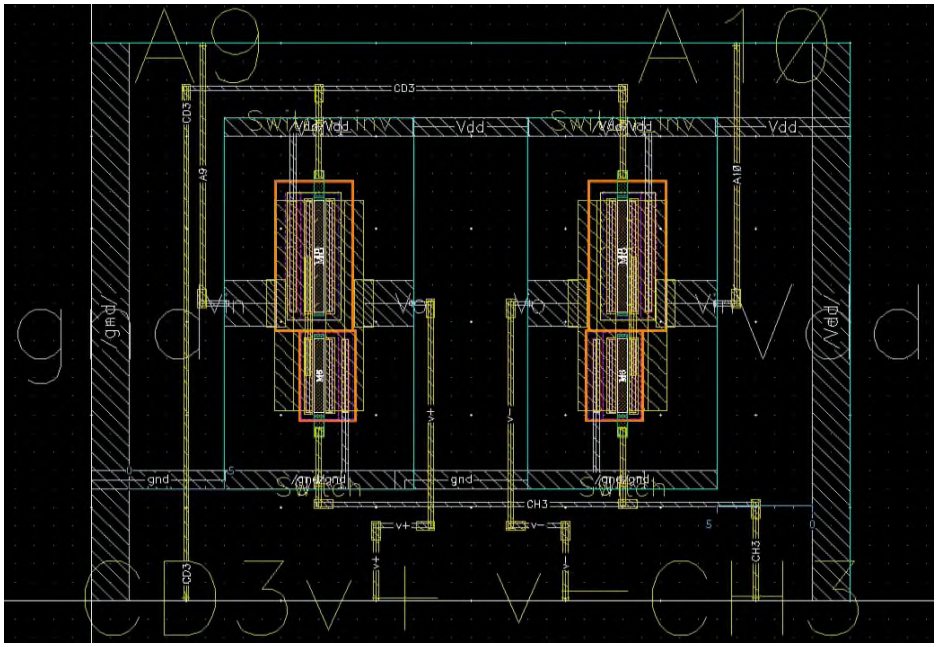

Figure 51: Channel 3 or 7 layout

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

4. Design of PAD Ring

In order to connect the circuits to the outside word a pad ring is required. The pad ring provides bonding pads to connect to the IC package, ESD protection circuits, and IO buffers for the digital circuits.

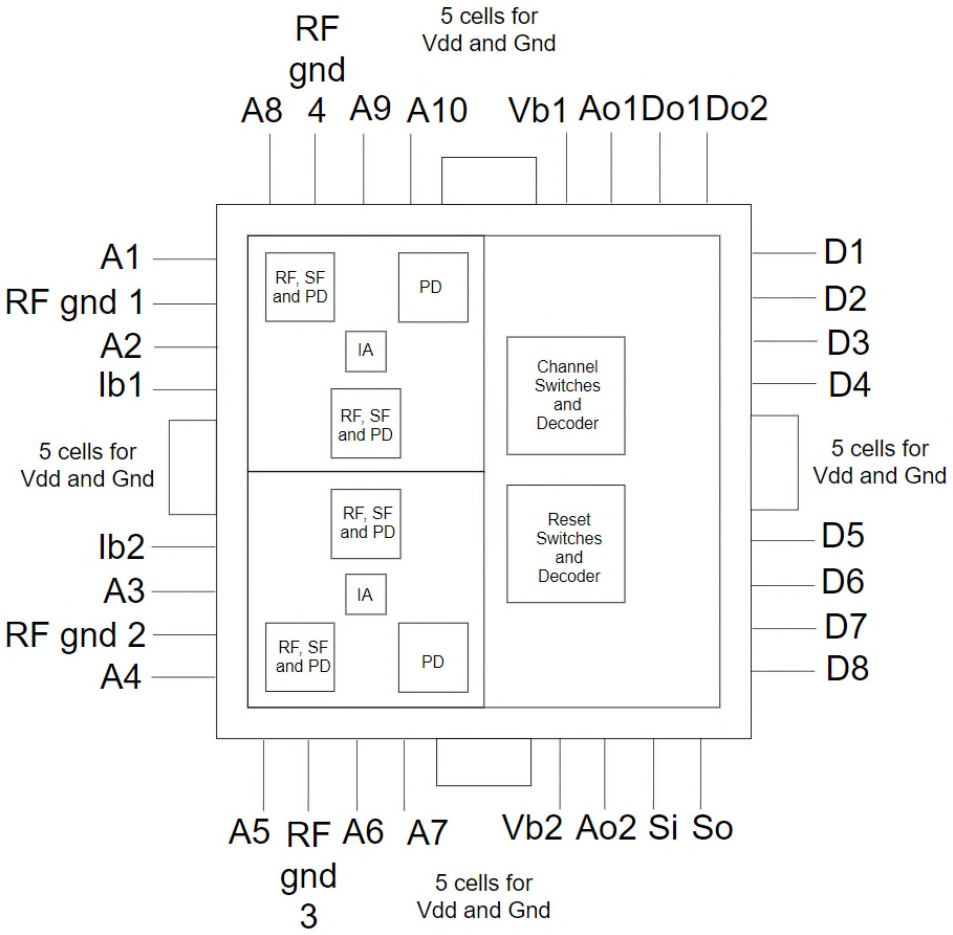

Figure 52: Floor Plan

As shown in Figure 52, the design has ten analogue input pins from A1 to A10 for channels 0 to 7, in which eight are single-ended inputs and two are differential input pins placed in a suitable location. And eight digital inputs from D1 to D8 towards the right, for reset and channel decoder. Also, there are two analogue outputs Ao1 & Ao2, two bias voltage pins Vb1 & Vb2, two current bias pins Ib1 & Ib2, and four RF grounds. Further, there are few test pins such as Si & So for test switch and Do1 & Do2 to test decoder output.

Each side of the PAD ring will have 13 I/O cells, in which 5 I/O cells are allotted for power supply and ground (VDD5, VDDR, VDDO, GNDO, and GNDR) on each side. In total 52 I/O cells lead to 52 pins for the package.

All the I/O cells used in the PAD ring are connected as shown in the schematic shown in Figure 53. We have 52 I/O cells same as the standard 52 card deck. For better differentiation between

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

each side, we have named Diamond for left, Club for right, Spade for top, and Heart for the bottom as shown in Figure 53. The final PAD ring layout is shown in Figure 54.

1.13 Schematic

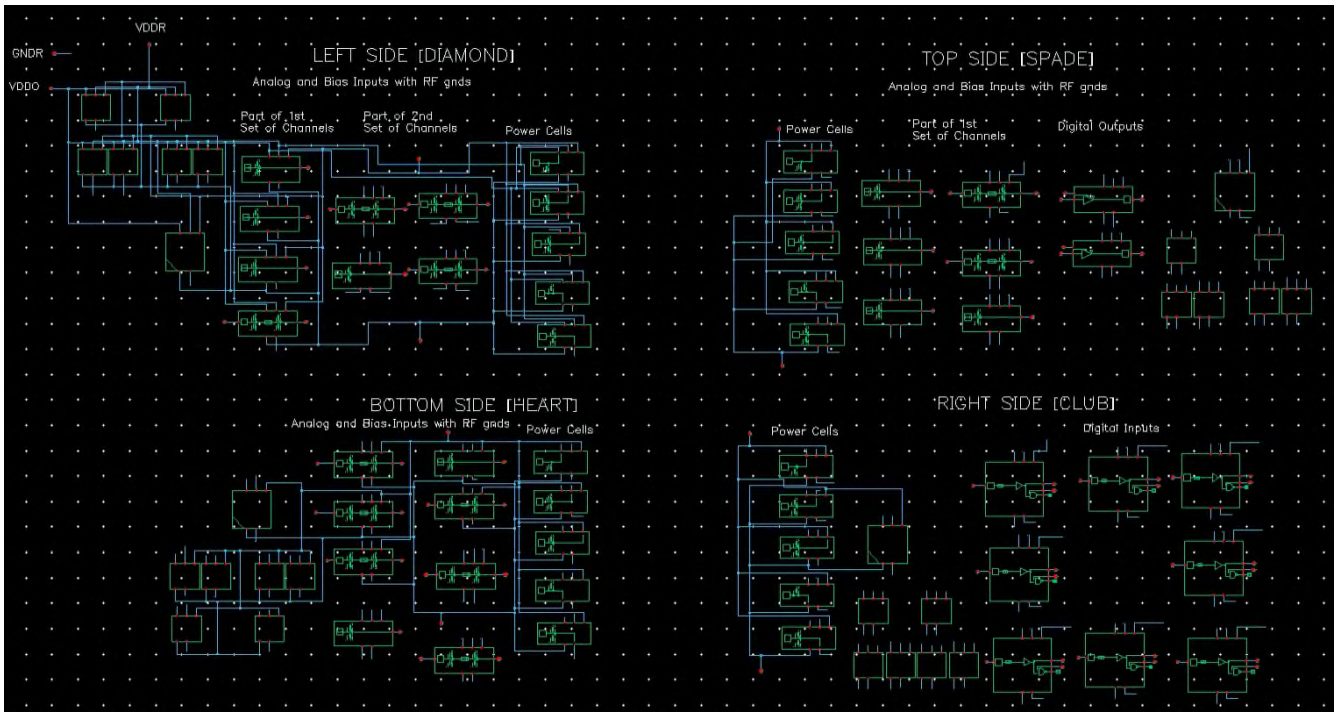

Figure 53: PAD ring Schematic

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

1.14 Layout

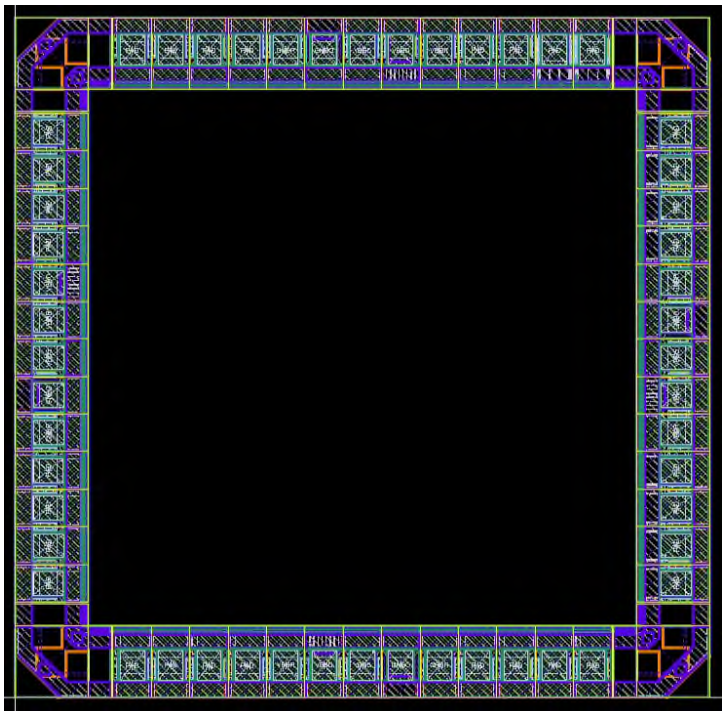

Figure 54: PAD Ring Layout

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

5. Overall System Schematic and Layout Simulation Results

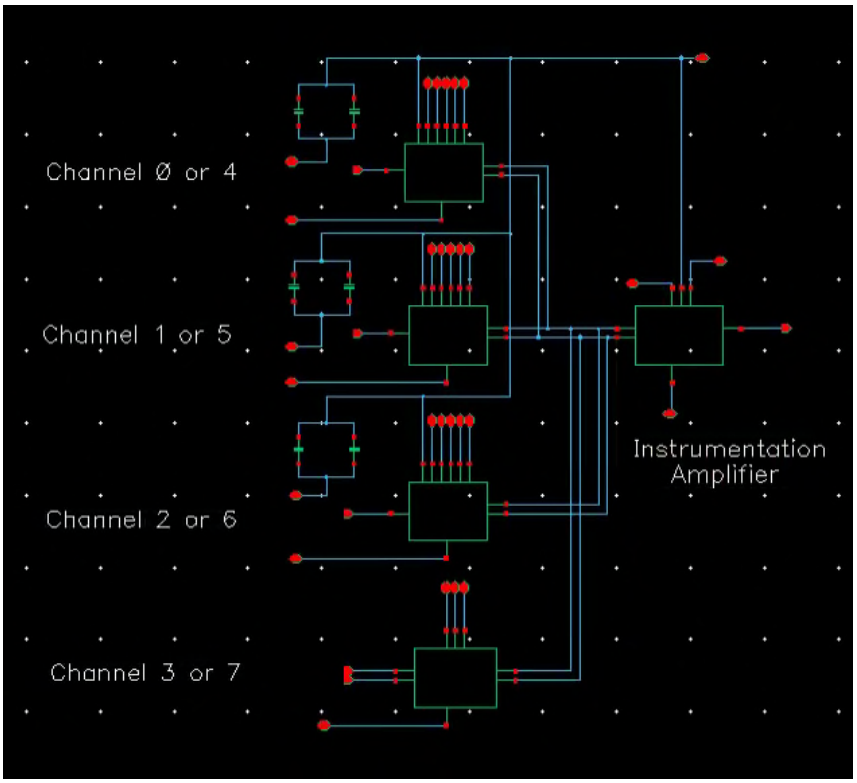

Figure 55: Channel 0 to 3 or Channel 4 to 7 Schematic

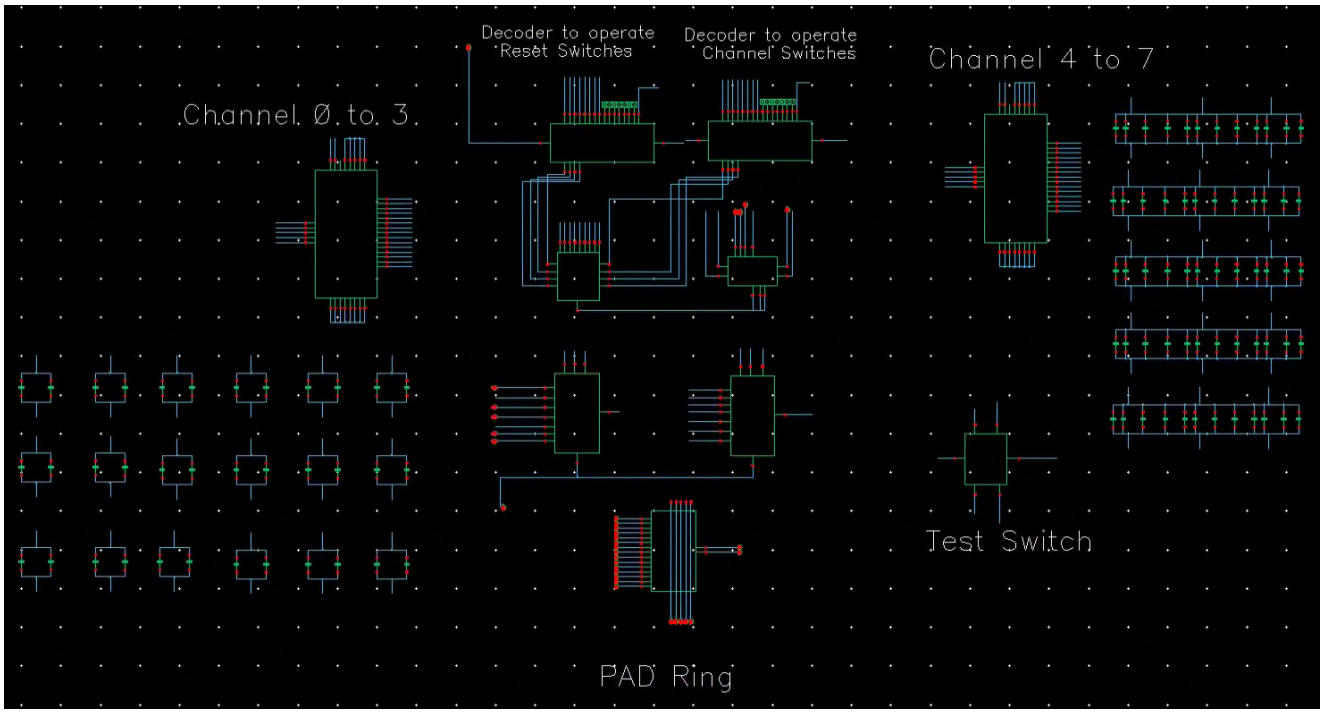

Figure 56: Overall System Schematic

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

Figure 55 shows the schematic of all the channels from 0 to 3 or 4 to 7 combined, which will be used in the overall system schematic as a symbol as shown in Figure 56. The overall system schematic shows all the blocks connected to the PAD ring with a bunch of decoupling capacitors connected between power and ground.

To increase the capacitance between the power supply and ground, decoupling capacitors are added in the chip space not required for other circuits. These decoupling capacitors will help to suppress the high-frequency noise in power supply rails. At high frequencies these capacitors will bypass the power supply providing a low impedance path between power and ground and also reduces the power rail coupling between the circuits fed from the power supply. As shown in Figure 57, a power gridding technique is used in the overall layout design to reduce the supply rail impedance. The longer the distance between the power supply and decoupling capacitor higher will be the noise.

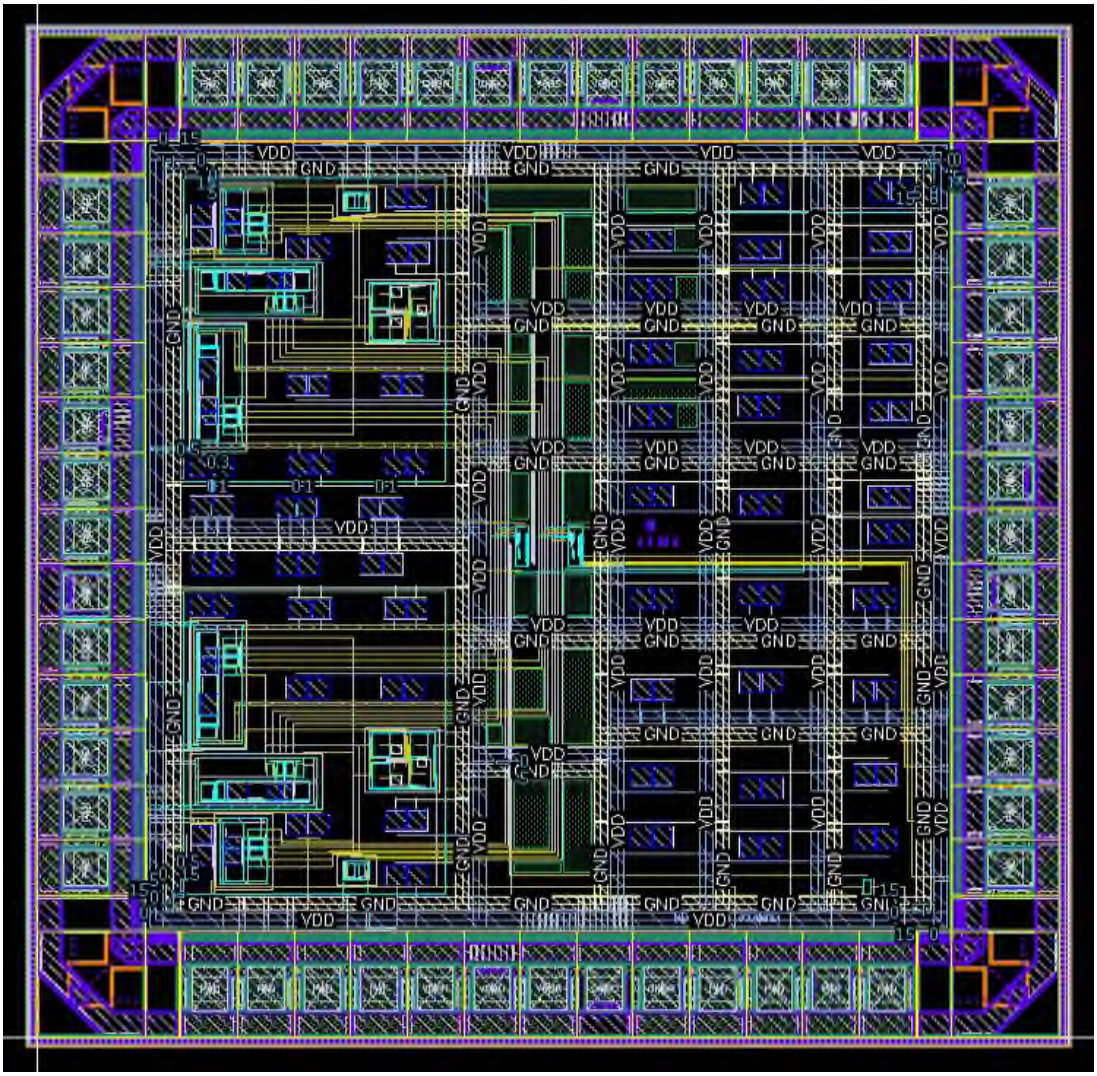

Figure 57: Overall System Layout

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

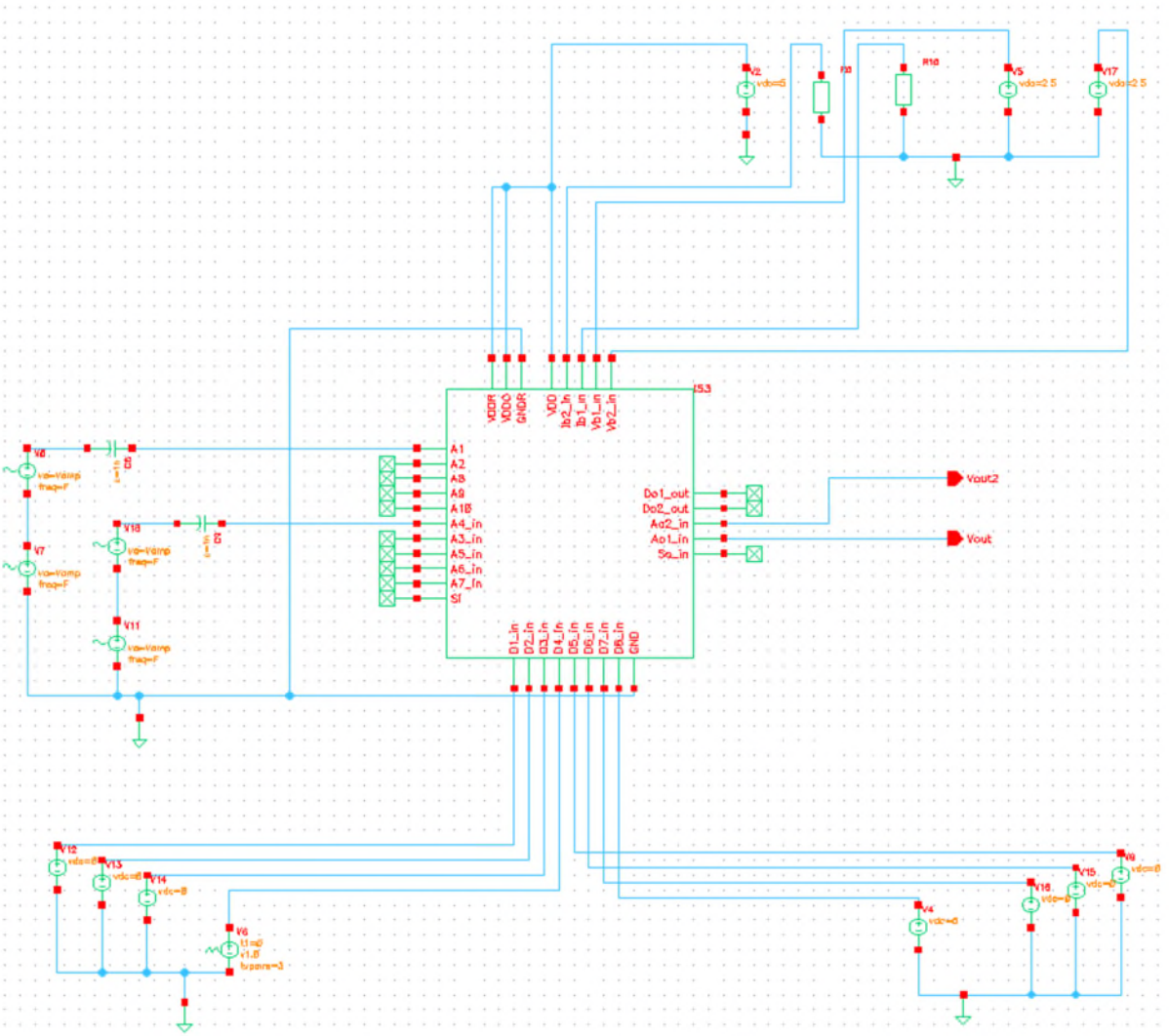

Figure 58: Test Bench for Overall System

Pins towards the left in Figure 58 are the input pins where we feed each channel with analog signals. On the right side, we have output pins where we measure output signals from two Instrumentation Amplifiers, Test Switch, and Decoder test pin. On the bottom side, we have digital input signal pins for 3 to 8 line decoders to control reset switches and channel switches. Towards the top, we have pins for voltage bias, current bias, and power signals for the entire chip. Channels 0 & 4 operate simultaneously since their switches are connected to the same output pins of the decoder. Similarly, channels 1 & 5, 2 & 6, and 3 & 7 are connected to the same output pins of the decoder respectively for simultaneous operation. However, channels 0 to 3 and channels 4 to 7 have different outputs connected through different Instrumentation Amplifiers (hence the two output Vout and Vout2).

1.15 Channel RF Transient Response

In order to test the each detector based input channel (0-2 and 4-6), a 2 µs rf burst was applied to each input after a 10 µs delay, and the differential detector output, and instrumentation

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

amplifier output was observed as the detector capacitor charged. At 13 µs the detector reset switch was operated to reset the detector. Each of the test results compares the schematic layout simulation with that obtained when the parasitic layout elements are included (post-layout simulation).

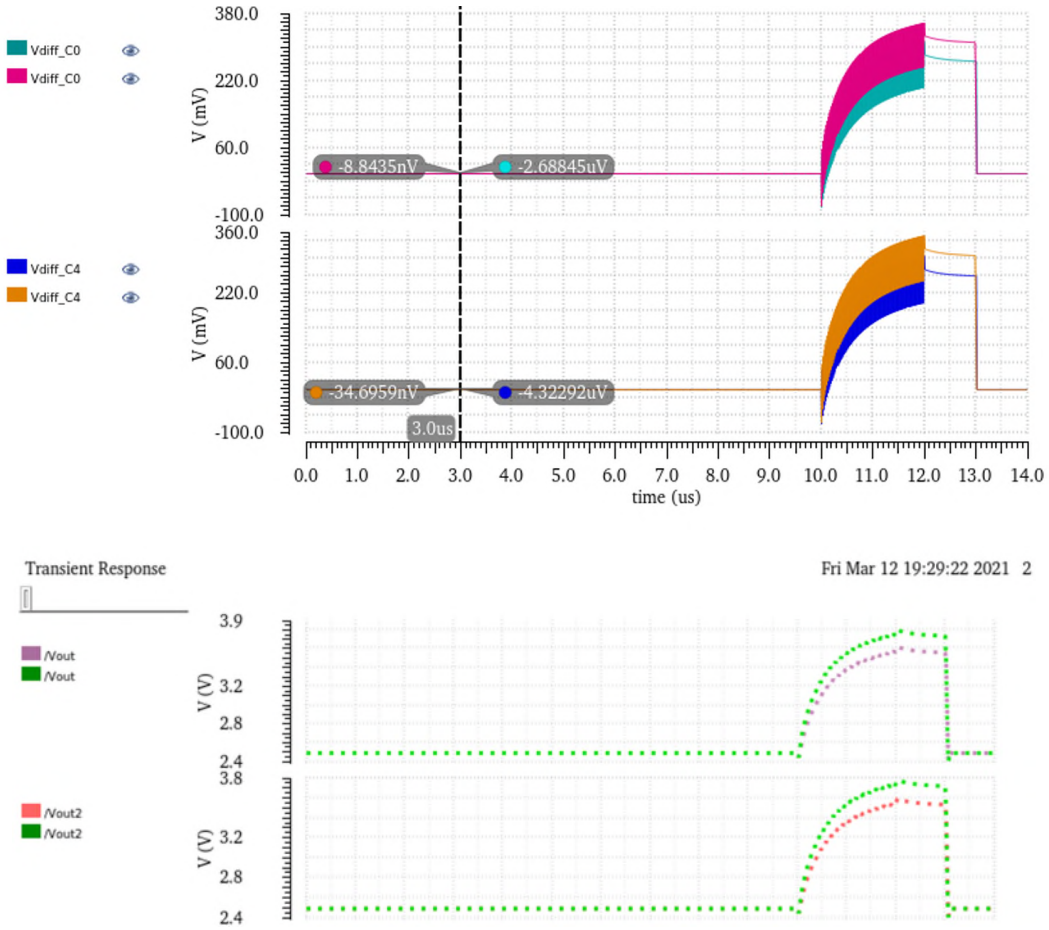

Figure 59: Transient Response of Channels 0 and 4 Schematic (larger amplitude) and Post layout (reduced amplitude) for Vin=50mV, Freq=50 MHz, vdiff (Vx-Vy) is the differential output at the Peak Detector; Vout and Vout2 are the outputs of the Instrumentation Amplifiers.

Figure 59 shows the results for channels 0 and 4 and Figure 60 shows the results for channels 1 and 5. It can be seen that the post-layout performance has a slightly lower sensitivity due to the capacitance and resistance of the interconnections, which are not included in the schematic simulation.

Figure 61 shows the rf transient results for channels 2 and 5. Again it can be seen that the post-layout performance has a slightly lower sensitivity due to the capacitance and resistance of the interconnections, which are not included in the schematic simulation.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

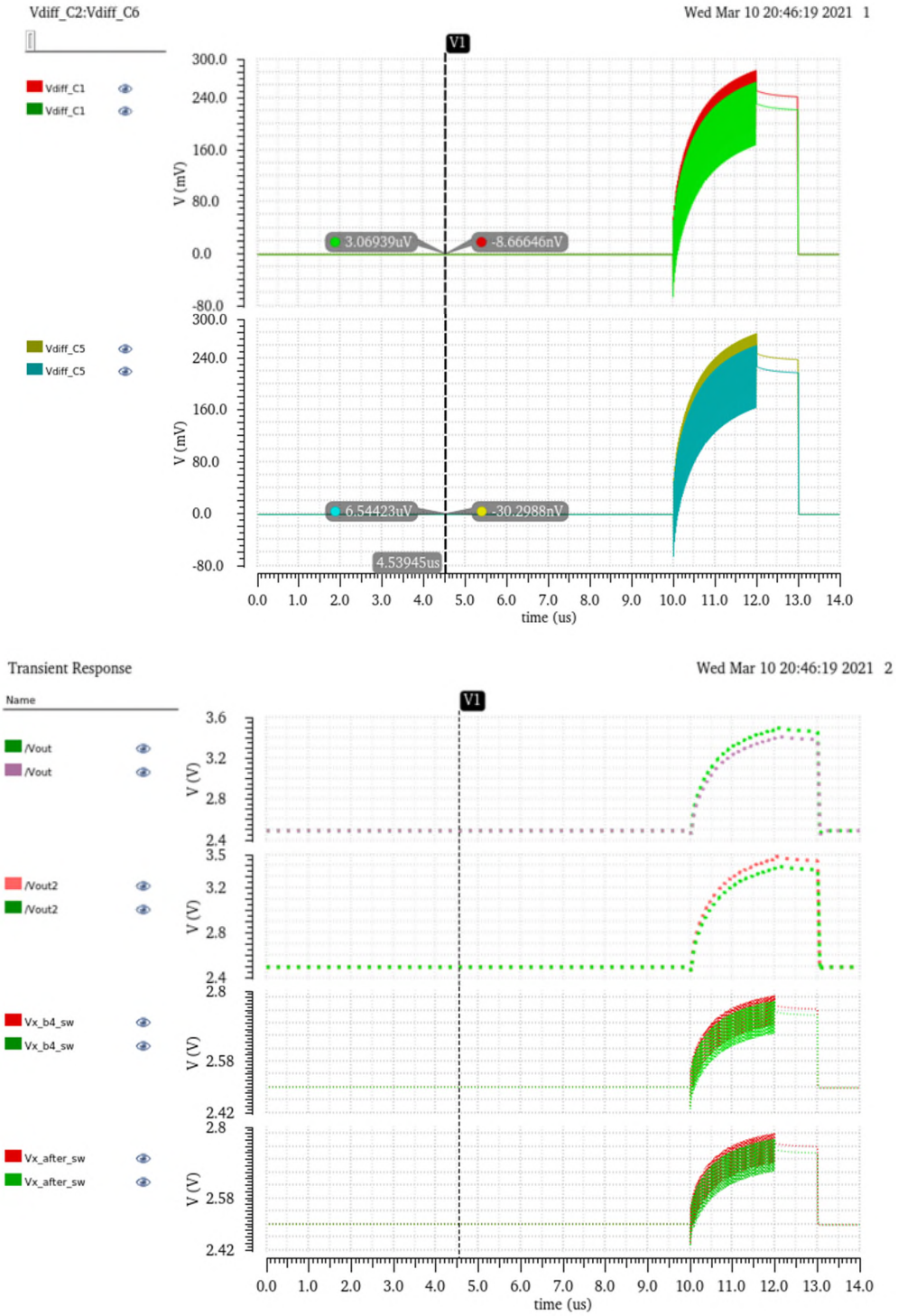

Figure 60: Transient Response of Channel 1 and 5 Schematic (larger amplitude) and Layout (curve with a slight drop), Vin=100mV, Freq=50 MHz, vdiff (Vx-Vy) is the differential output at the Peak Detector, Vout and Vout2 is the output at two Instrumentation Amplifiers. [Note: Vx_b4_sw= output of PD before switch, Vx_after_sw= output of PD after switch]

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

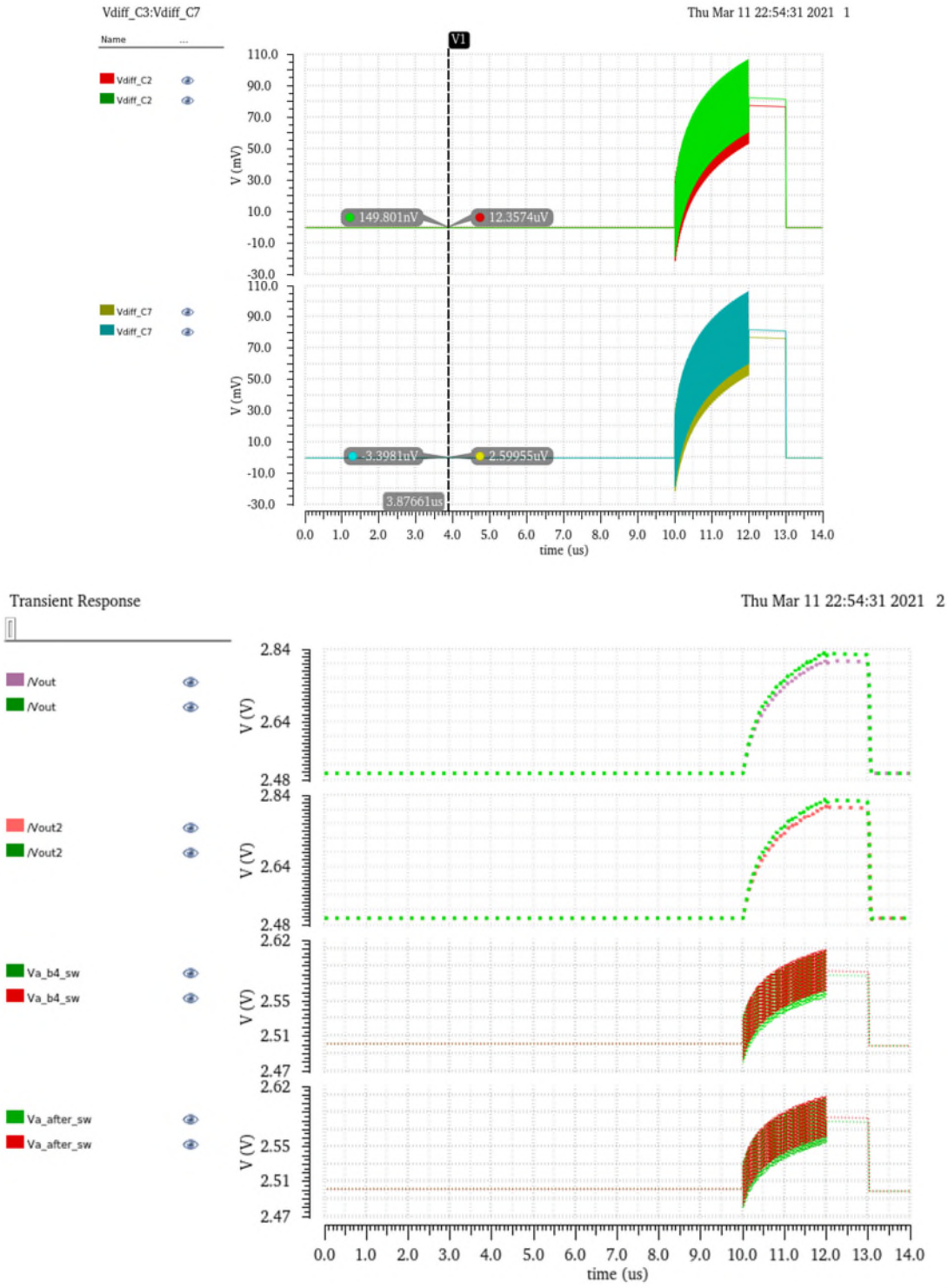

Figure 61: Transient Response of Channel 2 and 6 Schematic (larger amplitude) and Layout (curve with a slight drop), Vin=100mV, Freq=50 MHz, vdiff (Vx-Vy) is the differential output at the Peak Detector, Vout and Vout2 are the output at the two Instrumentation Amplifiers. Vx_b4_sw is the output of PD before the analogue multiplexer switch and Vx_after_sw it the output of PD after the switch

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

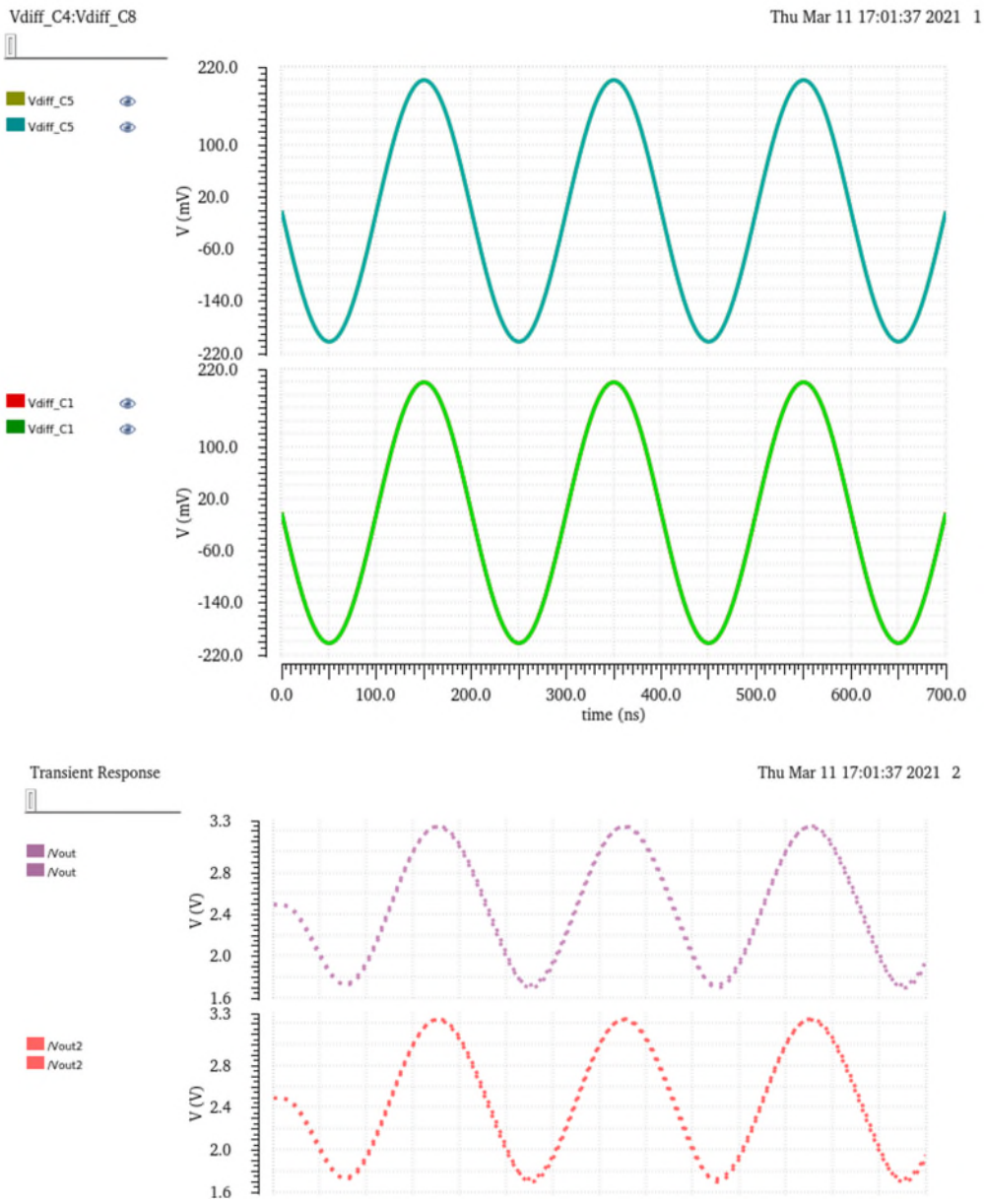

Figure 62: Transient Response of Channel 3 and 7 Schematic and Layout, Vdiff is the differential input to the Instrumentational Amplifier, Vout and Vout2 is the output at two Instrumentation Amplifiers.

Channels 3 and 7 connect to the differential inputs of the differential amplifier via the analogue multiplexer switches so a low frequency sine-wave is used for a transient test. The results are shown in Figure 62.

1.16 Frequency Response of RF amplifiers

The small signal frequency response of each rf amplifier, including the source follower, and loaded by the detector, is shown below. In each case the schematic and post-layout simulations are compared. Figure 63 and Figure 64 show the channel 0 and 4, high gain rf amplifier responses. Figure 65 and Figure 66 show the channel 1 and 5, broadband rf amplifier responses.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

In each case it can be seen that the added parasitics of the interconnect result in a reduction in operating bandwidth.

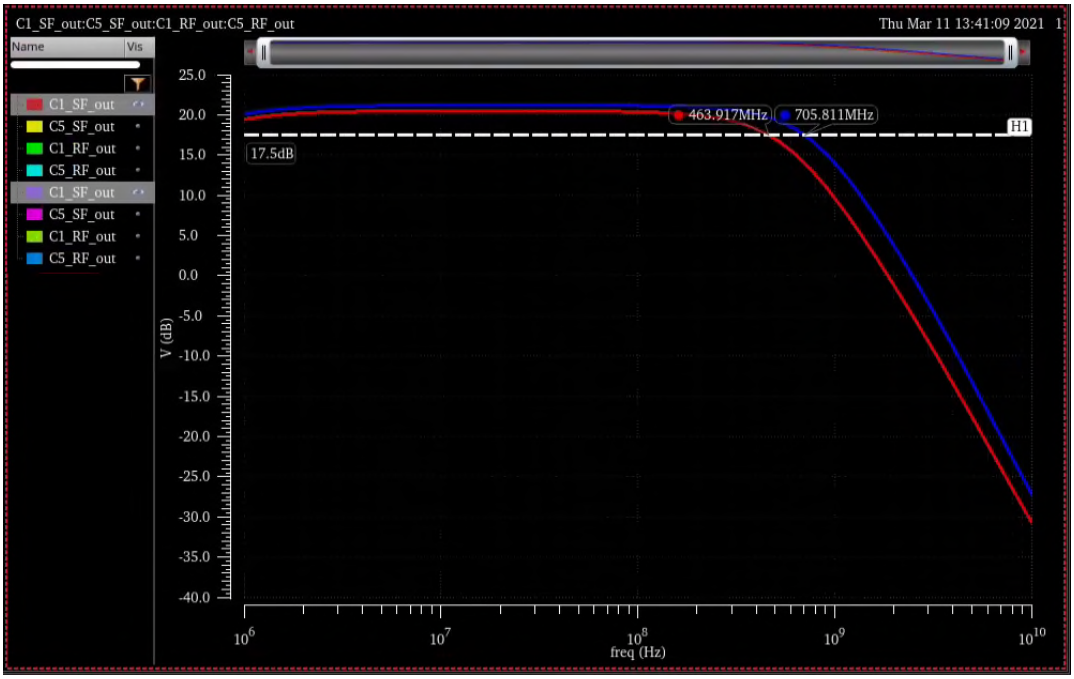

Figure 63: Channel 0 Schematic (Blue) and Post Layout (Red) Simulation with 1.20GHz RF amplifier: 463.91MHz (20.51dB), which has an analogue input pad with low series resistance.

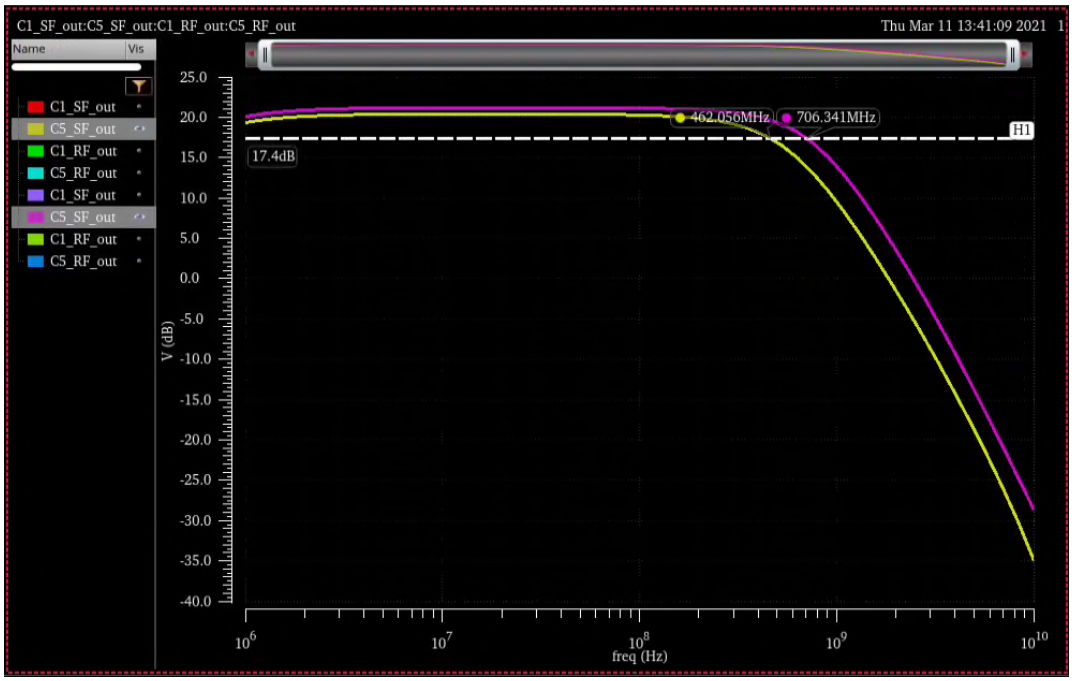

Figure 64: Channel 4 Schematic (Pink) and Post Layout (Yellow) Simulation with 1.20GHz RF amplifier: 462.05MHz (20.4dB), which has an analogue input pad with 100 ohm series resistance.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

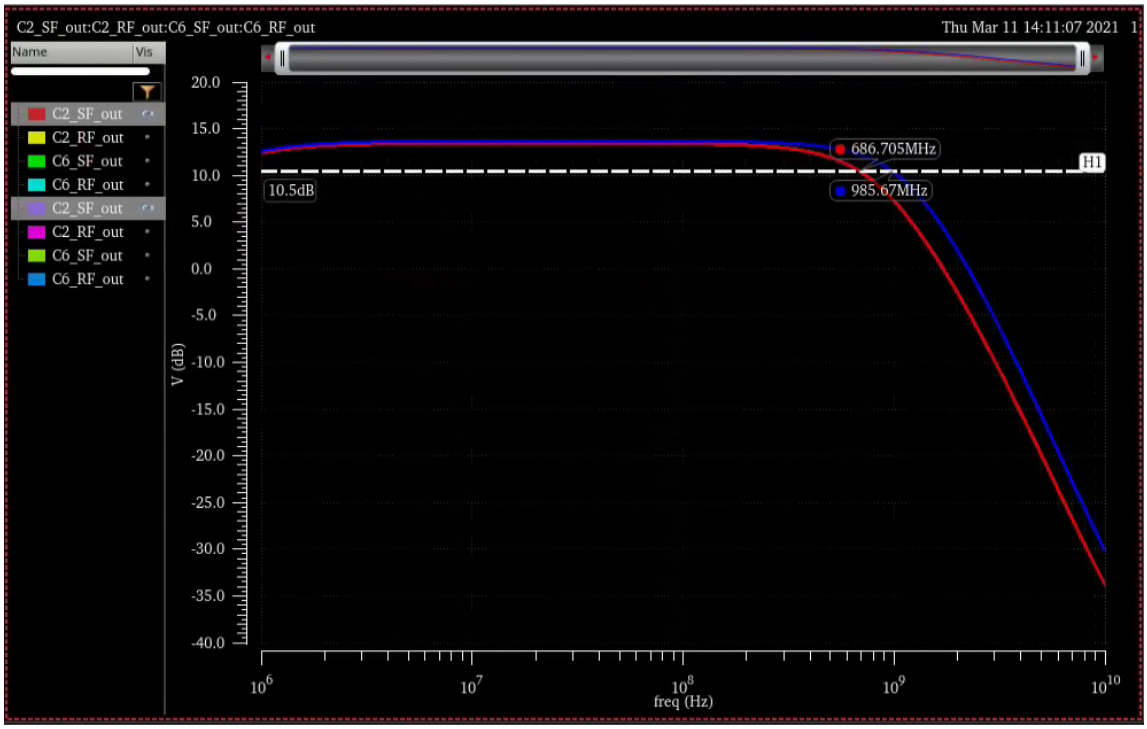

Figure 65: Channel 1 Schematic (Blue) and Post Layout (Red) Simulation with 2.25GHz RF amplifier: 686.70MHz (13.51dB), which has an analogue input pad with low series resistance.

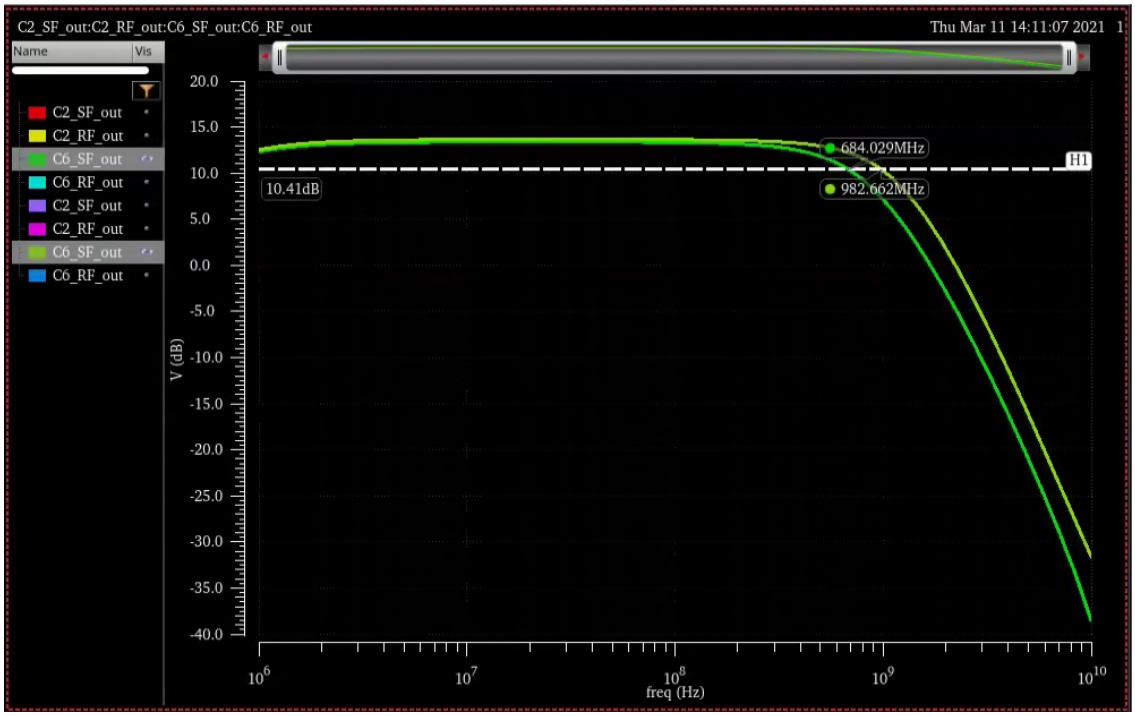

Figure 66: Channel 5 Schematic (Yellow) and Post Layout (Green) Simulation with 2.25GHz RF amplifier: 684.02MHz (13.41dB), which has an analogue input pad with 100 ohm series resistance.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

1.17 Decoder Test Simulation

Some 3-8-line decoder simulation results are show with test waveforms to exercise the logical function are shown below. Figure 67 shows the input test waveforms for the analogue multiplexer, and detector reset decoders. Figure 68 and Figure 69 shows the corresponding output waveforms for the two decoders, for the schematic, and post layout simulations.

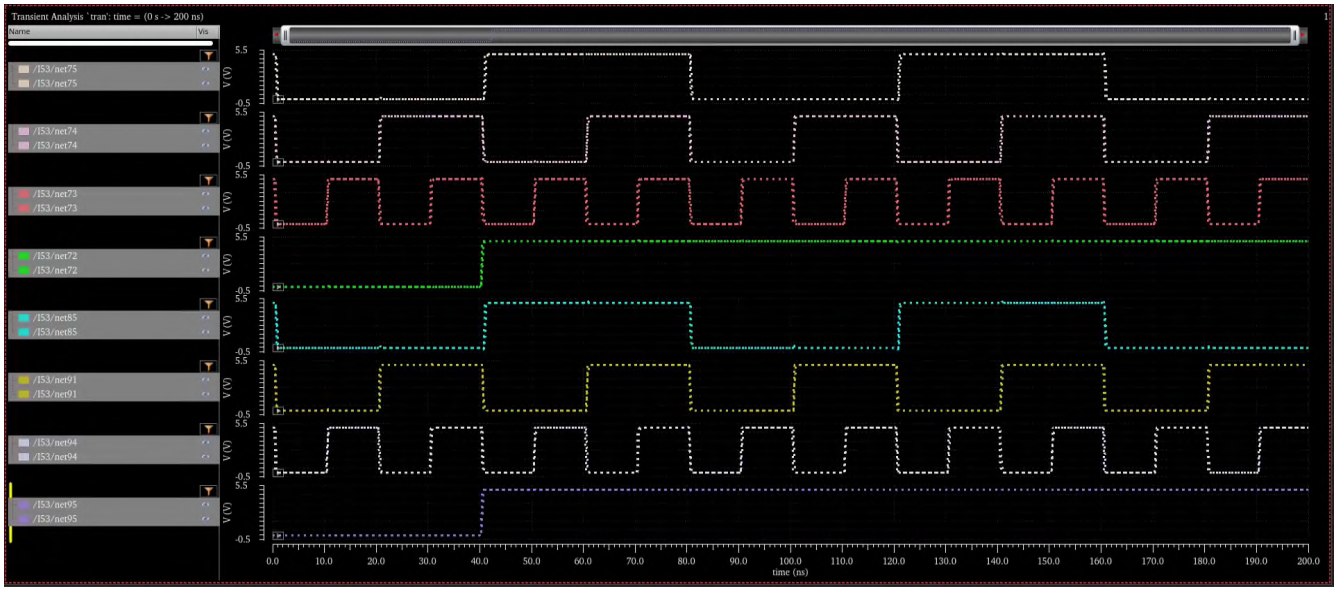

Figure 67: Input to the Reset Decoder (top four curves A,B,C and E respectively) and Channel Decoder (bottom four curves A,B,C and E respectively)

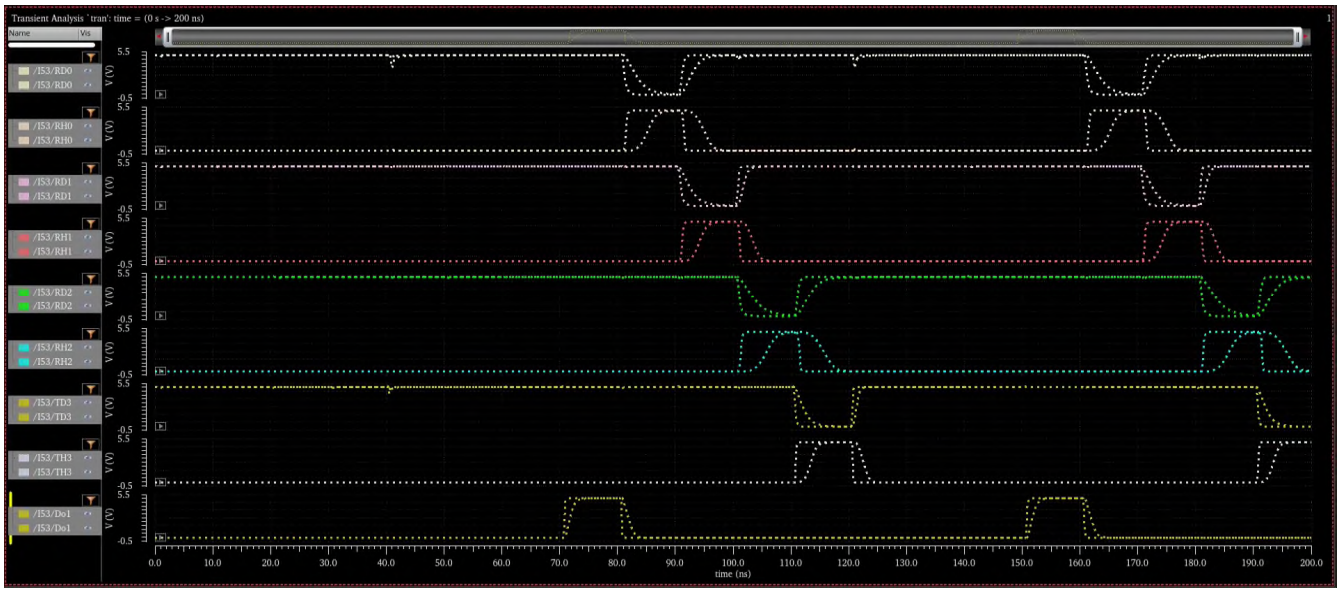

Figure 68: Output of the Reset Decoder, comparison between schematic (larger amplitude) and post-layout (curve with some delay) simulation.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

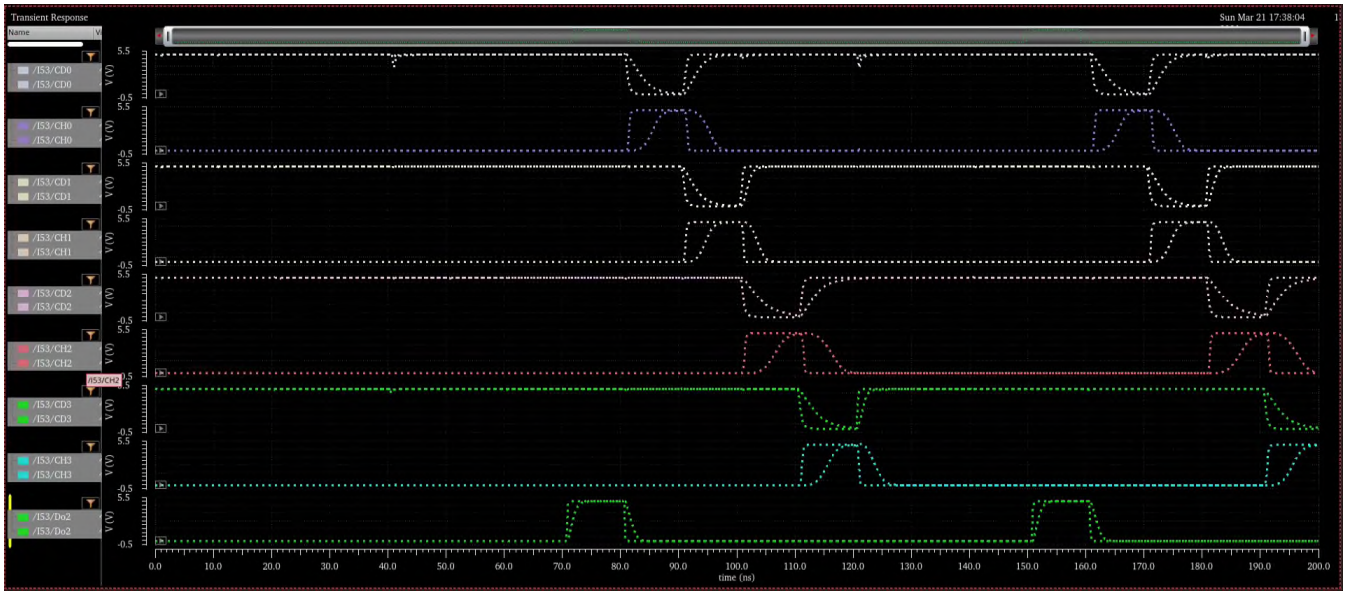

Figure 69: Output of the Channel Decoder, comparison between schematic (better curve) and post-layout (curve with some delay) simulation.

It can be seen that the parasitic elements of the interconnections slow down the logic edge rates. However, as we expect to switch between channels at a much lower rate, this is not a significant issue.

6. Conclusion and Future Work

The main goal of this deliverable was to complete the design of the IC detector to measure absorbed energy before March 31st, 2021. We have successfully completed the design of the IC detector in X-FAB XT018 0.18u HV SOI CMOS technology [13] using the Cadence Virtuoso design system [14] and the chip has been submitted to tape-out on March 29th, 2021 to Europractice mini@asic run from X-FAB. Physical IC is expected after 6 months from the submission date.

Meanwhile, during the lead time taken for IC fabrication, we will design a PCB test bench for our IC detector and will start writing a paper on the design. Once the IC is ready for testing, it opens the path to verify and validate the probability of susceptibility of on-board electronic components.

7. References

[1] D. A. Hill, M. T. Ma, A. R. Ondrejka, B. F. Riddle, M. L. Crawford, and R. T. Johnk, "Aperture excitation of electrically large, lossy cavities," *IEEE Transactions on Electromagnetic Compatibility*, vol. 36, no. 3, pp. 169–178, Aug. 1994, DOI:10.1109/15.305461.

[2] I. Junqua, J. P. Parmantier, and F. Issac, "A Network Formulation of the Power Balance Method for High Frequency Electromagnetic Coupling Applications,"

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

Interaction Notes, no. IN576, Nov. 2002, Available: http://ece-research.unm.edu/summa/notes/Interaction.html.

[3] I. D. Flintoft, S. J. Bale, A. C. Marvin, M. Ye, J. F. Dawson, C. Wan, M. Zhang, S. L. Parker, and M. P. Robinson, "Representative Contents Design for Shielding Enclosure Qualification From 2 to 20 GHz," *IEEE Transactions on Electromagnetic Compatibility*, vol. 60, no. 1, pp. 173–181, 2018.

[4] J. F. Dawson, A. C. Marvin, M. Robinson, and I. D. Flintoft, "On the Meaning of Enclosure Shielding Effectiveness," in *2018 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2018, pp. 746–751, DOI:10.1109/EMCEurope.2018.8485121, Available: http://eprints.whiterose.ac.uk/130815/.

[5] I. D. Flintoft, S. L. Parker, S. J. Bale, A. C. Marvin, J. F. Dawson, and M. P. Robinson, "Measured Average Absorption Cross-Sections of Printed Circuit Boards from 2 to 20 GHz," *Electromagnetic Compatibility, IEEE Transactions on*, vol. 58, no. 2, pp. 553–560, Apr. 2016, DOI:10.1109/TEMC.2016.2515658, Available: http://eprints.whiterose.ac.uk/93314/.

[6] M. Ramdani, E. Sicard, A. Boyer, S. Ben Dhia, J. J. Whalen, T. H. Hubing, M. Coenen, and O. Wada, "The Electromagnetic Compatibility of Integrated Circuits – Past, Present, and Future," *IEEE Transactions on Electromagnetic Compatibility*, vol. 51, no. 1, pp. 78–100, 2009, DOI:10.1109/TEMC.2008.2008907.

[7] A. H. Venkateshaiah, H. Xie, J. F. Dawson, A. C. Marvin, L. Dawson, and M. P. Robinson, "Coupling of Energy Into PCB Traces in a Reverberant Environment: Absorption Cross-section and Probability of Susceptibility," in *2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2020, pp. 1–6, DOI:10.1109/EMCEUROPE48519.2020.9245804.

[8] H. Xie, J. F. Dawson, A. C. Marvin, and M. P. Robinson, "Numerical and Analytical Analysis of Stochastic Electromagnetic Fields Coupling to a Printed Circuit Board Trace," *Electromagnetic Compatibility, IEEE Transactions on*, vol. 62, no. 4, pp. 1128–1135, Aug. 2020, DOI:10.1109/TEMC.2019.2954303, Available: http://eprints.whiterose.ac.uk/154302/.

[9] C. Scheytt, "Circuit and System Design, Fast Integrated Circuits For Digital Communication and Integrated Circuits For Wireless Communications," University of Paderborn, 2018.

[10] F. Najmabadi, "6 Cascode Amplifiers and Casode Current Mirrors," in *ECE102*, Perdue University, 2012, Available: https://www.academia.edu/40139694/6_Cascode_Amplifiers_and_Cascode_Current_Mirrors.

[11] A. S. Sedra, *Microelectronic Circuits*, 5th ed. New York ; Oxford: Oxford University Press, 2004.

[12] D. R. H. Phillip E. Allen, *CMOS Analog Circuit Design*. Oxford University Press, 2012.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

[13] "EUROPRACTICE | X-FAB." EUROPRACTICE, Mar-2021, Available: https://europractice-ic.com/mpw-prototyping/asics/x-fab/.

[14] "Virtuoso Analog Design Environment." Cadence, Mar-2021, Available: https://www.cadence.com/en_US/home/tools/custom-ic-analog-rf-design/circuit-design/virtuoso-analog-design-environment.html.

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/