A Comparative Performance Analysis of 6T & 9T SRAM Integrated Circuits: SOI vs. Bulk

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***Abstract*—This paper evaluates the performance of 6T & 9T static random access memory (SRAM) cells, for data stability and power metrics, with the aim to compare silicon-on-insulator (SOI) and bulk CMOS technologies. Each SRAM topology was designed & simulated in 180 nm 5 V XFAB-SOI and AMS-bulk processes, using optimized parameters and compatible devices. The fundamental variables analyzed were read noise margins, write trip current & voltage as well as leakage current (LC) and static power dissipation (SPD) under process and temperature (PT) variations. The static noise margin (SNM) butterfly curve and N-curve methodologies were used to assess the mentioned parameters. Compared to bulk technology, the SRAM cells designed with SOI were found to have lower SPD & LC, higher data stability, lower write ability, larger sensitivity to process variations and higher resilience to temperature deviations.**

***Index Terms*—SRAM, SOI, bulk, SNM, N-curve, PT**

I. Introduction

ELECTROMAGNETIC compatibility (EMC) characterization of integrated circuits (ICs) is of considerable importance as the high-speed signals cause signal & power integrity issues, resulting in interference problems [1]. Particularly, with the rapid pace of ICs technologies to reduce their dimensions and power consumption, they are more susceptible to conductive EM disturbances, and consequently, maintaining improved EMC characteristics has become much more challenging [2].

The speed of microprocessors primarily depends on the cache memory that it incorporates, which is predominantly consists of static random access memory (SRAM) cells [3]. The SRAM stores each bit by using bi-stable latching circuitry [4]. The measure of data stability of the SRAM is defined by the static noise margin (SNM), which is the minimum voltage noise that can flip its state [5]. A larger SNM ensures that the contents of the cell are unaltered during the read access, while allowing the cell to rapidly change its state across the write operation. In chip design, these conflicting requirements are overcome by balancing the relevant aspect ratios. Up to 70% of the systems on chip (SoC) area is occupied by embedded memories, which can limit the reliability improvement [6].

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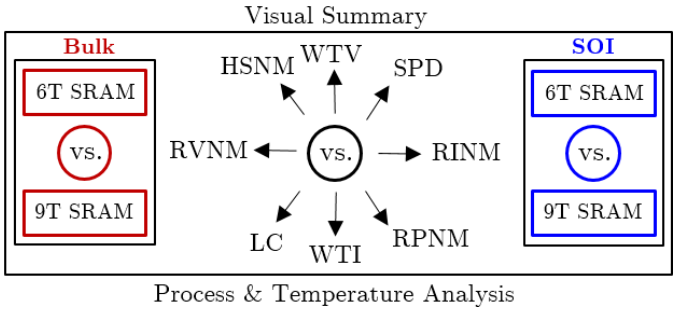

The main concerns for the SRAM cell design include maintaining a higher data stability as well as a lower power dissipation and leakage current. A suitable technology for such characteristics is the silicon-on-insulator (SOI) CMOS process. Compared to the bulk process, SOI has a thin buried oxide layer between the substrate, eliminating parasitic capacitances [7]. ICs designed with SOI can have faster performance, lower switching losses and higher integration [8].

Different topologies are adopted for SRAMs [10], but the most conventional implementations in industry are the six-transistor (6T) and nine-transistor (9T) cells. The former comprises MOSFETs which can store 1-bit of data with minimum aspect ratios, whereas the latter has a higher data stability and lower power consumption at the expense of occupying a larger area leading to a smaller package density [9]. In literature, to the best of the author's knowledge, there exists several works reporting the stability and performance of different architectures of SRAM cells designed in various nanometer bulk CMOS technologies [11]–[13]. However, those designs have not yet been implemented in SOI benefiting from reduced substrate losses and withstanding harsh environments (e.g. high temperature and humidity).

Take-Home Messages:

- SRAM cells as the integral part of cache memories are prone to read and write failures. Worst case stress (temperature and process) scenarios for these operations must be analyzed.
- Compared to bulk, SRAM cells designed in SOI technology have lower power consumption & leakage current as well as higher endurance to temperature but are more susceptible to process variations.
- Compared to the conventional 6T SRAM, the 9T SRAM cell show better data stability and power metrics, when implemented in SOI in contrast to bulk.

In this paper, both 6T & 9T SRAM cells were designed and simulated in 5 V 180 nm SOI and bulk technologies. Process & temperature (PT) variation simulations were carried out on both SRAM cells in each technology to comparitively study their performance. Parametric analysis was performed at extreme corners with the aim to show robustness of SRAM cells in SOI compared to bulk under extreme conditions, sweeping the relevant electrical parameters such as current, voltage and power noise margins, static power dissipation and leakage current. The voltage and current transfer characteristics were monitored using the SNM butterfly curve and the N-curve metric, respectively.

The paper is organized as follows. Section II describes the peripheral components schematics and setup configurations of the SRAM cells. Section III reports on the extensive analysis of the simulation results, while concluding contributions of this study are presented in Section IV.

II. Materials and Methods

This section introduces the 6T & 9T SRAM cell's principle of operation followed by the description of the stability metrics. Both cells were simulated in bulk and SOI CMOS 5 V using 180 nm technology kits, provided by AMS and XFAB foundries, respectively. A similar logic gate size was found in the design kit of each foundry and the SRAM cells were configured to have the same dimensions with a minimum MOSFET length of 700 nm. All circuits were designed using Cadence Virtuoso and the simulations were obtained in Spectre.

A. Design and Description of 6T & 9T SRAM cells

A conventional 6T SRAM, shown in Fig. 1(a), works in three modes of operations: read, write and hold. It contains two cross-coupled inverters forming a latch with two access transistors to read and write the data stored in the memory cell [14]. The load and drive transistor pairs make up the inverter. The SRAM cell was designed to provide an effective read operation and an acceptable write margin. The cell is written by driving the desired value and its complement into the bit line (BL) and bit line-bar (BLB) when the word line (WL) is enabled. For reading data, the two bit lines are pre-charged to a floating state and once the WL is raised, the appropriate bit-line is pulled down while the other remains high.

For a proper read operation, the access and drive NMOS transistors are sized such that the value of voltage rise at the node never exceeds the threshold value for the other inverter [15]. The cell ratio is the aspect ratio of the drive with respect to the access transistors. A higher value results in a better data stability; it is kept at 3.0 for all circuits. Similarly, ensuring proper write operation requires access and PMOS load transistors to be sized so that a zero may be written into the cell. The pull-up ratio is the aspect ratio of the load to the access transistors, which determines the write ability of the SRAM. It is kept at 0.20 for all circuits, so that they are easily writable.

During the hold mode, the WL is disabled, consequently switching off the access transistors. This results in the load

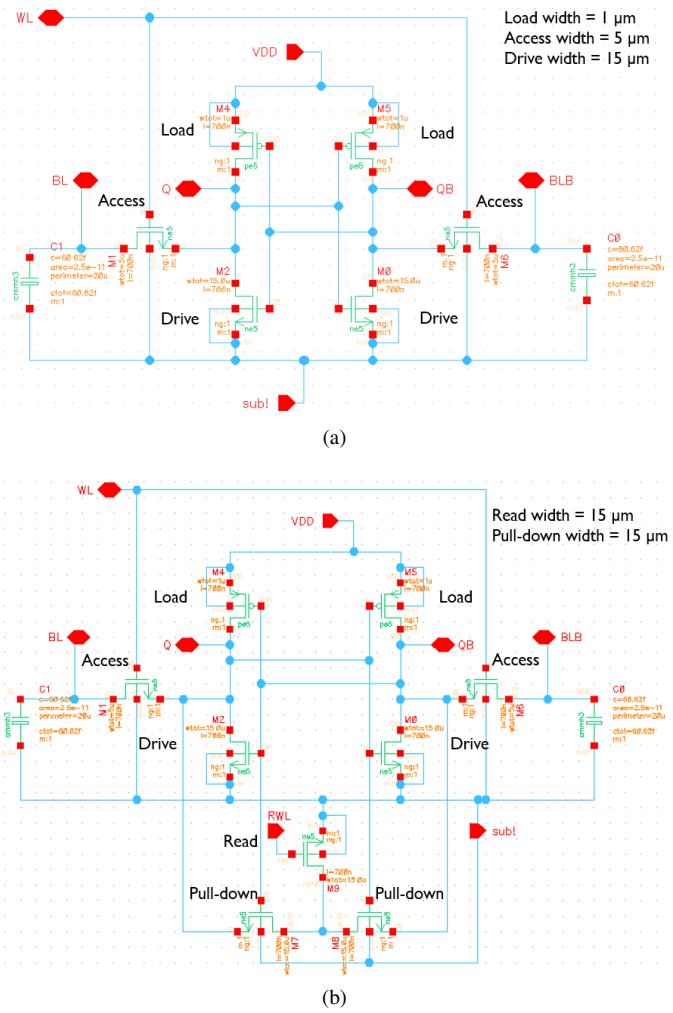

Fig. 1. Schematic of SRAM cell designed in Cadence: (a) 6T; (b) 9T.

transistors continuing to reinforce each other and the contents of the coupled latch remain unchanged until the supply voltage (VDD) remains on. In a standard memory block of an IC, the pins Q and QB of the SRAM cell are connected in parallel to a sense amplifier which pulls the desired data. Additionally, there are row and column decoders which select the appropriate cell where the data is written or read [16].

The designed 9T SRAM cell, shown in Fig. 1(b), employs a differential read operation for better read access times. Its operation differs from the 6T SRAM, where the three added transistors create a strong pull-down effect in the read mode [17]. The aspect ratios of the read and pull-down transistors are identical to the drive-NMOS to maitain symmetry and decrease switching losses. When the read word line (RWL) is enabled, the differential pull-down of the drive transistors results in a less resistance between data storage nodes to ground. When the RWL is disabled, it behaves as a 6T SRAM in the write and hold mode. However, since the extra transistors are switched off, the leakage current is reduced.

B. Static Noise Margin (SNM)

It helps to determine the data stability of the SRAM cell. It is modelled by plotting the butterfly curve and measuring the

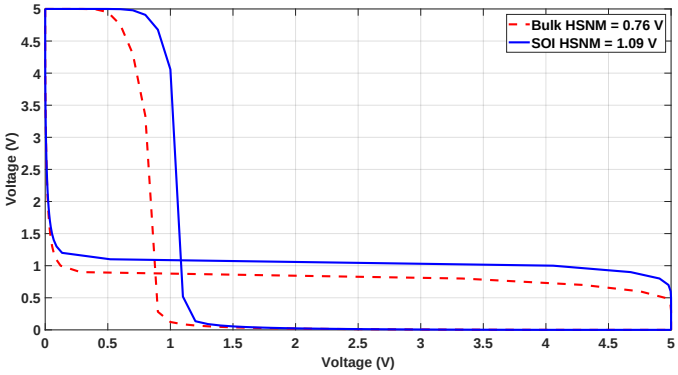

Fig. 2. SOI vs. bulk: HSNM of 6T & 9T SRAM cells.

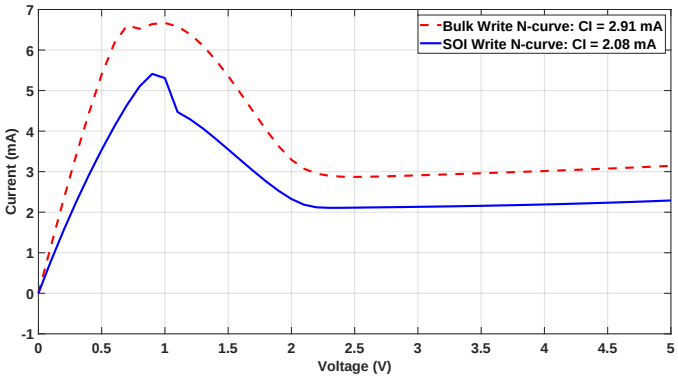

Fig. 3. SOI vs. bulk: write N-curve metric of 6T & 9T SRAM cells.

side of the longest square created between the cross-coupled inverters [18]. For the considered SRAM cells, the SNM was monitored at the Q and QB output pins by subjecting the inputs of the inverter circuits to two equal and opposite independent DC voltage sources ranging from 0 V to 5 V. The disadvantage of measuring the SRAM stability through the SNM metric is that it does not support the characterization of the supply current and the write ability.

C. N-curve Metric

It is used for inline testers and provides information about the current and voltage in a single plot [19]. In the simulation setup, an independent DC voltage was connected between the QB and ground pins. The DC voltage sweep was performed and the supply current, voltages and power were monitored for each operational mode of the SRAM. These results were extended to power metrics from which the data stability and write ability of the SRAM is calculated. The variables derived from the N-curve are the following:

- read current noise margin (RINM) & read voltage noise margin (RVNM) indicate the peak current and the maximum tolerable voltage, which can alter the contents of the SRAM cell in read mode.
- write trip current (WTI) & write trip voltage (WTV) are the minimum current and voltage required to write data into the SRAM and are found from the read N-curve.
- critical current (CI), derived from the write N-curve, is needed to write data in the SRAM cell without failure.

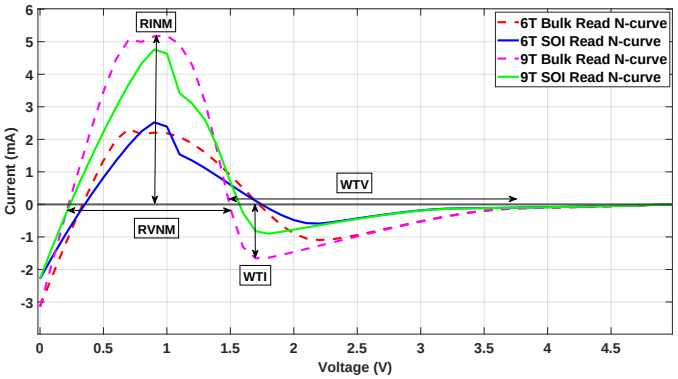

Fig. 4. SOI vs. bulk: read N-curve metric for 6T & 9T SRAM cells.

- read power noise margin (RPNM), the product of the RINM & RVNM, shows the highest power necessary to make the SRAM fail to read the data.

D. Leakage Current & Static Power Dissipation

The major problem with SRAM cell design is the rise in leakage current (LC) and the resulting static power dissipation (SPD), which are increasingly becoming a significant source of the total power consumption [21]. SOI technology lowers the junction capacitances and allows the circuits to work at a more reduced power preserving identical speeds [20]. Lower power dissipation and leakage current seem to be the most distinguished advantage SOI has over bulk. For all SRAM circuits, the LC is measured between the supply voltage and ground while all the access MOSFETS are turned off, retaining data for a particular period of time. The SPD is calculated from the leakage current and the variation in power supply.

III. Simulation Results and Discussion

This section presents all DC sweep, transient, process and temperature parametric simulations related to the 6T & 9T SRAM circuits in 5 V 180 nm bulk and SOI. The transient simulations were timed to 1 μs. The voltage for DC simulations was swept from 0 V to 5 V with a step size of 0.1 V. While the nominal temperature is 27 °C, the temperature ranges for PT simulations are −40 °C to 80 °C with 5 °C steps. The lowest temperatures recommended by both foundries are identical (−40 °C) whereas the highest temperature for SOI and bulk are 175 °C & 80 °C, respectively. The latter was selected as the maximum temperature limit to have a fair comparison between both processes. For process variations only extreme corners, worst speed (WS) and worst power (WP), were considered and compared to the nominal (N) process.

A. Stability Analysis of 6T & 9T SRAM Cells: SOI vs. Bulk

The 6T & 9T SRAM circuits are identical during the hold and write operations. To characterize the SRAM cells designed in SOI and bulk, the hold SNM (HSNM) is plotted using the butterfly curve as seen in Fig. 2. The blue and red curves represent the HSNM for both 6T & 9T SRAM cells designed in SOI and bulk, respectively. It is observed that the HSNM

of the SOI SRAM (6T & 9T) surpasses that of bulk by 0.33 V. Even though both circuits have identical dimensions, the SRAMs designed in SOI perform more efficiently than bulk in the retention mode. The reason behind this is that the former has lower parasitic junction capacitances in its cross-coupled inverters [22].

For a comparison in the write mode, the write N-curve metrics of both 6T & 9T SRAM cells designed in SOI and bulk are plotted in Fig. 3. The parameter to analyze is the CI, which is monitored at the lowest peak of the curve before it becomes stable. A lower CI ensures that a smaller current is required to write the data into the SRAM without failure. The CI of the bulk SRAM (6T & 9T) is higher compared to that of SOI by 0.83 mA. The cause of this variation is that the sub-threshold voltage swing of the SOI MOSFETs is lower than bulk, resulting in a reduced gate current required for switching [23].

The significant difference between the 6T & 9T SRAM cells is in the read operation. Fig. 4 shows four distinct read N-curves for the SRAM cells designed in bulk and SOI at nominal conditions. It is evident that the RINM, RVNM, WTI and WTV parameters are higher for the 9T compared to the 6T for both SOI and bulk processes. These results prove that the 9T SRAM has better tolerance to DC noise as well as enhanced write ability than the 6T SRAM due to the isolation of the read current path by using MOSFETs of minimum feature size. However, the response of both SOI and bulk is divergent when it comes to the topology of the SRAM circuits. For the 6T SRAM, the SOI version has larger RINM & RVNM but lower WTI & WTV than the bulk version. This demonstrates that in the case of the 6T SOI SRAM, higher data stability is achieved with a lower write ability than bulk. Alternatively, for the 9T SRAM, the bulk version has a predominantly larger RINM, WTI & WTV but a smaller RVNM compared to SOI. To better analyze the results, the RPNM is calculated for all four circuits. The 9T SOI SRAM has the most significant value of RPNM among all circuits, which indicates the highest tolerance to DC noise during the read operation.

The values of LC and SPD are notably lower for SOI than bulk (6T & 9T) SRAM cells. This observation is due to the SOI process allowing fewer leakage effects and ensuring better power consumption. Whatever the technology, the 9T has a smaller LC & SPD in comparison to the 6T SRAM.

A summary of the results are given in Table I. The following observations were made:

- SRAMs designed with SOI has enhanced data stability and power metrics but a worse write ability than the bulk versions.
- 9T SRAM has better noise metrics than the 6T SRAM and combining it with SOI shows a more robust performance.

TABLE I
SOI VS. BULK: PARAMETERS OF 6T & 9T SRAM CELLS AT NOMINAL CONDITIONS (T = 27 °C, P = N)

Param.	6T SRAM (Bulk)	6T SRAM (SOI)	9T SRAM (Bulk)	9T SRAM (SOI)
RINM	2.32 mA	2.54 mA	5.17 mA	4.89 mA
RVNM	1.31 V	1.39 V	1.35 V	1.45 V
WTI	1.09 mA	0.64 mA	1.65 mA	0.98 mA
WTV	1.95 V	1.91 V	2.50 V	2.44 V
LC	2.73 µA	1.61 µA	1.45 µA	0.77 µA
RPNM	3.04 mW	3.53 mW	6.92 mW	7.09 mW
SPD	13.65 µW	8.06 µW	7.23 µW	3.82 µW

B. Process & Temperature (PT) Corner Analysis

PT variations can rapidly affect the sensitivity of the CMOS circuit performance. The process variations are the critical design parameters (die-to-die) in the semiconductor design technology that precisely controls the functionality of the design at the nanometre level [24]. These include film thickness, impurity concentration densities, lateral dimensions and diffusion depths. These variations causes a mismatch, which results in a reduced yield of SRAM arrays in different technologies.

All circuits have temperature variations because of the power consumption linked to the switching of the CMOS transistors. A rise in temperature will reduce the mobility, threshold voltage and increase the propagation delay of the MOSFETs. However, the temperature surge will also result in the faster switching of the transistors and accelerate performance [25]. This will impact the voltage and current noise margins for the SRAM cells. Therefore, a PT corner analysis is performed on both 6T & 9T SRAM designs in SOI and bulk CMOS technologies to compare the effects.

A DC parametric simulation was performed on each SRAM circuit with extreme temperature and process variations while keeping the supply voltage constant at 5 V. Only at four specific corners reasonable changes in the stability parameters of each design were observed. C1 & C3 corners characterize the effect of extreme temperatures only and the C2 & C4 show the combined effect of process and temperatures for each SRAM cell. Here follows a summary of the obtained results given in Table II to Table V.

Monitoring C1 & C3 shows that the RINM, RVNM, RPNM, WTI & WTV are inversely proportional to temperature for all SRAM cells. The rise in temperature increases mobility and reduces the threshold voltage of individual MOSFETs, thus, resulting in a lower noise margin and trip voltages for bulk & SOI processes. When comparing both the topologies (Table II & Table IV), the read noise margins and write trip metrics for 9T SRAM cells are more impacted by temperature than the 6T SRAM cells. The reason is that the former has more NMOS transistors leading to a higher variation in the differential pull-down effect. An interesting observation is that the deviation of these stability parameters is more prominent in bulk than SOI versions of the 6T & 9T SRAM circuits (Table II & Table III). This demonstrates that, compared to bulk technology, the SRAM cells designed in SOI are more resilient to DC noise and write failure when subjected to

TABLE II
6T SRAM BULK PARAMETERS CHANGE WITH PT

Param.	T = -40 °C P = N (C1)	T = -40 °C P = WS (C2)	T = 80 °C P = N (C3)	T = 80 °C P = WP (C4)
RINM	3.61 mA	3.68 mA	1.49 mA	1.44 mA
RVNM	1.41 V	1.47 V	1.25 V	1.22 V
WTI	1.52 mA	1.25 mA	0.87 mA	0.99 mA
WTV	2.26 V	2.11 V	1.62 V	1.74 V
LC	2.02 µA	1.94 µA	3.85 µA	3.91 µA
RPNM	5.09 mW	5.40 mW	1.86 mW	1.76 mW
SPD	10.11 µW	9.70 µW	19.39 µW	19.62 µW

TABLE III
6T SRAM SOI PARAMETERS CHANGE WITH PT

Param.	T = -40 °C P = N (C1)	T = -40 °C P = WS (C2)	T = 80 °C P = N (C3)	T = 80 °C P = WP (C4)
RINM	3.11 mA	3.69 mA	2.12 mA	1.44 mA
RVNM	1.46 V	1.44 V	1.37 V	1.23 V
WTI	0.78 mA	0.66 mA	0.59 mA	0.63 mA
WTV	2.01 V	1.94 V	1.87 V	1.90 V
LC	1.52 µA	1.10 µA	2.15 µA	3.06 µA
RPNM	4.54 mW	5.45 mW	2.90 mW	1.77 mW
SPD	7.60 µW	5.52 µW	10.75 µW	15.31 µW

TABLE IV
9T SRAM BULK PARAMETERS CHANGE WITH PT

Param.	T = -40 °C P = N (C1)	T = -40 °C P = WS (C2)	T = 80 °C P = N (C3)	T = 80 °C P = WP (C4)
RINM	7.53 mA	7.71 mA	4.00 mA	3.84 mA
RVNM	1.52 V	1.57 V	1.10 V	1.04 V
WTI	1.84 mA	1.67 mA	0.98 mA	1.05 mA
WTV	2.98 V	2.11 V	1.62 V	1.79 V
LC	0.93 µA	0.90 µA	1.99 µA	2.24 µA
RPNM	11.44 mW	12.10 mW	4.41 mW	3.99 mW
SPD	4.65 µW	4.48 µW	9.96 µW	11.13 µW

TABLE V
9T SRAM SOI PARAMETERS CHANGE WITH PT

Param.	T = -40 °C P = N (C1)	T = -40 °C P = WS (C2)	T = 80 °C P = N (C3)	T = 80 °C P = WP (C4)
RINM	5.56 mA	6.85 mA	4.14 mA	3.92 mA
RVNM	1.49 V	1.66 V	1.38 V	1.12 V
WTI	1.11 mA	1.67 mA	0.91 mA	1.05 mA
WTV	2.87 V	2.23 V	2.06 V	2.38 V
LC	0.62 µA	0.49 µA	1.23 µA	1.55 µA
RPNM	8.28 mW	11.371 mW	5.72 mW	4.40 mW
SPD	3.09 µW	2.46 µW	6.15 µW	7.74 µW

drastic temperature changes.

The LC and SPD parameters were found to increase for the SRAM circuits at the same corners with the temperature rise. This behavior is due to the decrease of the threshold voltage of NMOS transistors at higher temperatures, which leads to a substantial increase in gate leakage. As described previously, those mentioned parameters are higher for bulk compared to SOI. In contrast to SOI, there is an exponential surge in the LC & SPD of bulk 6T and 9T SRAM cells with temperature (Table II & Table IV). This is due to the fact that bulk does not have a buried insulation layer, which decreases the effect of temperature on leakage path associated with the drain and source of MOSFETs.

At corners C2 & C4, the combined effect of process and temperature is analyzed for all read noise margins and write trip parameters. As expected, RINM, RVNM & RPNM are inversely proportional to process and temperature for all four circuits (Table II). A faster process (WP) and greater temperatures result in quicker switching of the MOSFETs, escalating their mobility and further diminishing the threshold voltages. Contrarily, the WTV and WTI are either increased or decreased slightly at C2 & C4 corners, respectively, with the effects of process and temperature competing against each other. A quicker process (WP) improves the write ability of the SRAM cells. All read and write parameters of the SOI versions of the SRAM cells are more sensitive to process variations compared to bulk. The 9T SOI SRAM cell shows the highest variation with respect to process among all circuits due to the higher number of MOSFETs (Table IV).

As far as the LC and SPD are concerned at C2 & C4, the variation in SOI SRAM cells is higher compared to that in bulk. The power dissipation of the SOI version of the SRAM cells (6T & 9T) is less impacted by temperature and is more susceptible to process changes (Table III & Table V).

The read data stability, write ability and power metrics of the 6T & 9T SRAM cells designed in SOI are more resistant to changes in temperature and sensitive to process variations compared to bulk technology. The read parameters and power metrics are inversely and directly proportional to the combined process & temperature changes, respectively. Nevertheless, the write ability of all SRAM cells improves with a faster process. The read noise margins and power dissipations of 9T SOI SRAM are the most immune metrics to temperature changes. As far as the 6T bulk SRAM is concerned, it is the least susceptible to process variations among all schematics.

IV. CONCLUSION

With the aim to compare SOI and bulk processes, this paper investigates the data stability, write ability and power

metrics of 6T & 9T SRAM cells when exposed to process and temperature variations. Compared to bulk technology, the SRAM cells designed in SOI show better data stability, lower leakage supply current & power dissipation and a higher resilience to temperature changes. However, the SOI SRAMs have reduced write ability and greater sensitivity to process variations in comparison with bulk SRAMs. The SOI version of the 9T SRAM cell was found to have the best specifications among the circuits considered in this study, which makes it a promising approach to develop more robust SRAM structures.

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