A Comparison Among DPI Immunities of Multi-Stage CSVCOs and Ring Oscillators

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***Abstract*—This paper evaluates & compares, through electrical simulation, the immunity of multi-stage current starved voltage controlled oscillators (CSVCOs) and ring oscillators (ROs) submitted to direct power injection (DPI). All circuits were designed and simulated in the 180 nm 5 V XFAB-SOI process, with matching dimensions. The failure criteria selected were the output frequency, peak-to-peak voltage and DC offset voltage. Results demonstrated, that CSVCOs were sucsceptible at lower DPI frequencies, while the ROs were susceptible at higher frequencies. Both were impacted by different failure criterions. Regardless of the oscillator category, a higher number of inverter stages resulted in lower susceptibility to incident power levels. As a consequence of increasing the power level of RF injections, the highest DC supply current and output power, monitored for each oscillator was close to their nominal output frequencies. These circuits are currently being fabricated in a test chip and immunity measurements will be performed on it.**

***Index Terms*—Integrated Circuits, EMC, DPI, Susceptibility, VCO**

I. Introduction

One of the most formidable challenges for IC design companies is to avoid redesigning ICs. It is a high cost process and increases the time to market for the products. Electromagnetic interference (EMI) is one of the primary reasons to redesign ICs, which indicates the importance of considering electromagnetic compatibility (EMC) during the design process [1].

To investigate EMI problems at the design phase, CAD simulations can help if they are performed correctly and comply with the real cases [2]. Measurement methods are standardized by applying well-established EMC standards at the IC level. Moreover, models are needed at the simulation level.

Direct power injection (DPI) is an electromagnetic interference (EMI) immunity test for integrated circuits, defined in the IEC-62132-4 standard [3]. Radio frequency (RF) disturbance is injected into the pin of the IC. The forward power level of the signal is amplified until the functionality of the circuit fails according to the relative failure criteria. The recommended frequency range of the injected RF signal is from 150 kHz to 1 GHz. There are models for the DPI test setup in simulation which comply well with measurements [4]. Because of the simplicity of performing DPI, it is the most widely used IC level RF immunity test method [5].

Voltage controlled oscillator (VCO) is the vital component of the phase locked loop (PLL) and function generators. It is vital to study the performance of a multi-stage VCO and its susceptibility to conducted electromagnetic interference (EMI). In this paper, two conventional architectures were tested, a current starved VCO (CSVCO) and a ring oscillator (RO) with an output buffer.

The RO with an output buffer is a simple multi-stage inverter consisting of an odd number of delay cells. Its output frequency can only be controlled by the voltage supply and delay cell stages. The buffer is connected at the output stage for the stability of the signal. In contrast, for a CSVCO, the rise and fall times of the cell are regulated by externally biased MOSFETs through a biasing voltage. Thus, by controlling the voltage and sizing of the transistors one can maintain the desired frequency with a broad tuning range, occupy a compact area and consume less power than the RO [6].

The paper is organized as follows. Section II describes the DPI simulation setup and the characteristics of the multi-stage oscillators. Section III focuses on the extensive analysis of the simulation results when DPI is applied on the supply rail of each oscillator. The concluding contributions of this study are presented in Section IV.

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II. Materials and Methods

This section presents the DPI circuit's operation and test simulation, followed by the selected failure criteria. The PETER_ESEO research chip was designed using Cadence Virtuoso, and the simulations were obtained in Spectre. All multi-stage oscillators were included in a 1.52 × 1.52 mm test chip using a silicon-on-insulator (SOI) CMOS 180 nm 5 V technology. They are designed to have similar frequency ranges and matching aspect ratios. A parasitic extraction was performed for the IC, to better approximate the realistic behavior of the setup.

A. DPI Circuit & Test Setup Description

As shown in Fig. 1, the DPI circuit includes the RF source with a DC blocking capacitor, a decoupling network and a voltage supply with a DC choke inductor. It generates continuous wave (CW) RF disturbances at particular frequencies and power levels [7]. The parametrized characteristics of the generator are the incident power (P_{dpi}) , frequency of the input signal (F_{dpi}) and the delay before the start of the immunity test. For each circuit simulation, the delay is taken as half of the period of the output signal to give it time to settle [8].

The purpose of the DC blocking capacitor having a value of 6.8 nF according to [3], is to avoid any DC signal from being fed back into the RF source. The decoupling network consists of a 100 pF capacitor with its parasitic resistance and inductance. It decouples the power supply and represents the nominal environment for the IC to operate correctly. The biasing inductor, ensures that a high impedance path is created for the RF disturbances, so that they are not absorbed by the 5 V supply [9], [10].

An electrical model of the DPI testbench is presented in Fig. 2. It consists of the DPI circuit, the IC package, the switches, PETER_ESEO die, main power supply (V_{DD}) and ground. The chip, among other structures, includes 3-stage & 5-stage CSVCOs and ROs. It contains a padring with electrostatic discharge (ESD) protection structures to both the V_{DD} and ground. Each VCO has an isolated (V_{DD}) and a single separate ground, benefiting from SOI technology. The switches allows for individual injection of the RF signal into the supply pin of each oscillator and will not interfere with the other pins.

Additionally, the four CSVCOs and ROs are connected to a frequency divider (FD) digital circuit, which reduces the fundamental frequency of the output signal to be accurately measured at the analog output pin. The FD circuit is connected to the main power supply and is completely isolated from the DPI signal. The input pin (V_{in}) is only turned on when tuning the frequency of the CSVCO, while the frequency of the RO is pre-defined at the design stage by the delay cell. However, it is noticed that the output frequency of the latter is sensitive to the power supply voltage.

The package chosen for the test chip is a ceramic quad flat package (CQFP). It was modelled using the IC-EMC software [11], which aids to generate a realistic package model from mechanical information and computes the lumped parasitic elements.

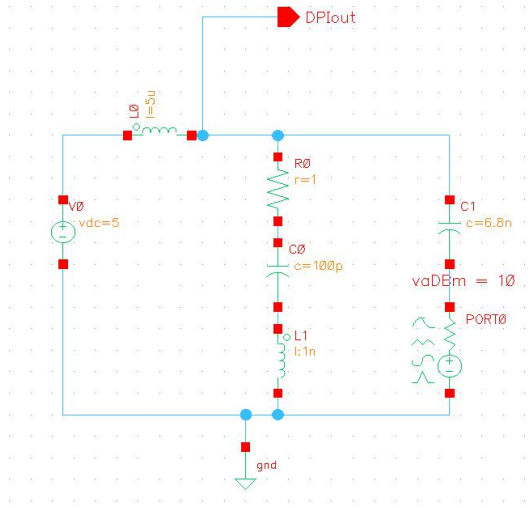

Figure 1. Schematic of the DPI Circuit.

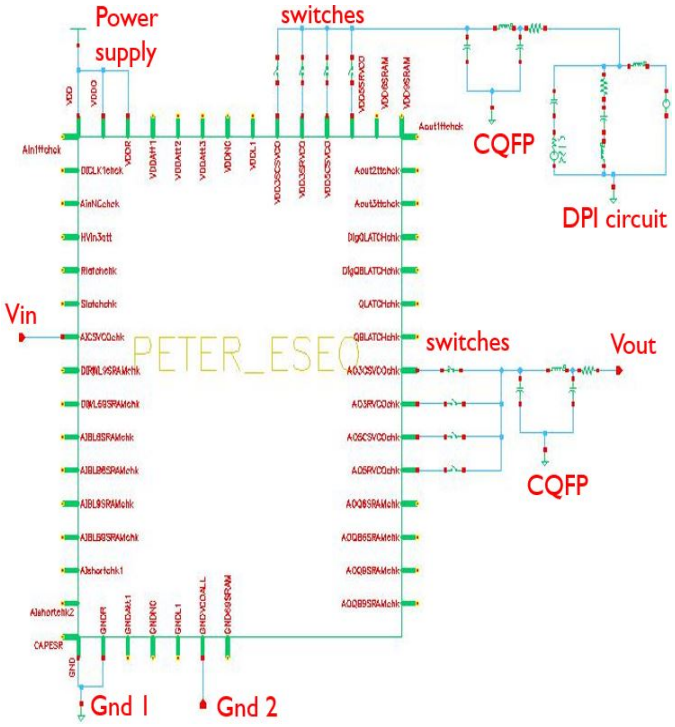

Figure 2. Schematic of the DPI test bench for the PETER _ ESEO chip.

B. Failure Criteria

The immunity criteria to monitor a failure of the oscillators for the DPI test are the following. If any one of the tolerance is reached, then the tested circuit would result in an overall FAIL.

- C1: ± 5 % deviation in frequency of the oscillator signal monitored at the analog output pin,

Table I
MULTI-STAGE CSVCOs & ROs CHARACTERISTICS

Type of Oscillator	VCO Operating Frequency	Frequency Divider (FD)	Output Frequency (C1)	Peak to Peak Voltage (C2)	DC Voltage (C3)
3 Stage CSVCO Vin= 1.8V	703 MHz	8 (FD=3)	87.9 MHz	5.35 V	2.65 V
3 Stage RO with buffer	955 MHz	8 (FD=3)	79.5 MHz	5.81 V	2.92 V
5 Stage CSVCO Vin= 1.6V	271 MHz	4 (FD=2)	68.1 MHz	5.67 V	2.80 V
5 Stage RO with buffer	815 MHz	16 (FD=4)	50.8 MHz	5.69 V	2.83 V

- C2: ± 10 % deviation in the peak-to-peak voltage (V_{p-p}) measured before the FD,
- C3: ± 10 % deviation in the DC offset voltage observed before the FD.

The failure criterion commonly used to characterize the conducted EM immunity of analog circuits is the RF-induced average DC-shift [12]. Since, the VCO is driving a divider input, the variation of the output V_{p-p} becomes crucial as well. Furthermore, the parameter that affects the stability of an oscillator is the frequency of the output signal, which needs to be constant. Taking this into consideration all tolerance limits selected were similar to industry standards. Table I illustrates the characteristics of the multi-stage CSVCOs & ROs at their nominal values.

III. SIMULATION RESULTS AND DISCUSSION

This section describes and compares the susceptibility tables of the oscillators and their respective output power. All transient simulations were timed to 2 μs since it covers the minimum frequency of the RF source. F_{dpi} was swept between 1 MHz and 1 GHz using 50 MHz steps. At each frequency point P_{dpi} was increased from 1 dBm to 37 dBm with a step size of 3 dBm, until the circuit failed according to any of the selected criterions. Once a failure occurs, all higher power levels were considered as a FAIL and the frequency increments to the next point. This was performed to avoid any meaningless artifacts in the simulation results, the circuit being considered defective as soon as a failure occurs. Each DPI simulation has a time delay before the RF signal is injected, for the circuit to reach a stable operating point. In the case of CSVCOs, the tuning input (V_{in}) is maintained constant during the whole simulation.

A. Analysis of Susceptibility Tables

The aim of a DPI simulation is to extract a susceptibility table and provide the designer a preliminary image about the EMC behavior of the IC. It shows what frequency and power levels can intefere with the functianality of the circuit under test [13]. In the simulation phase not all frequency and power steps were covered, but the selected step sizes were sufficient to examine the behavior of the CSVCOs & ROs under DPI.

The susceptibility table of the 3-stage CSVCO shown in Fig. 3 (a) was examined first. It was observed that the minimum P_{dpi} = 13 dBm, at which the 3-stage CSVCO failed, was at F_{dpi} = 100 MHz. The circuit was more immune to DPI at higher frequencies, malfunctioning at P_{dpi} = 28 dBm. Most of the FAILs in the table at lower F_{dpi}, were caused by the deviation in the V_{p-p} (C2), while the output frequency (C1) remained constant. This is due to the architecture of the CSVCO, as the RF signal initially disturbs the biasing transistors, triggering a change in the frequency, before eventually reaching the inverter stage. However, the V_{p-p} of the CSVCO was susceptible to DPI, at smaller F_{dpi}. The variation in the DC offset voltage (C3) had only an impact on the failure at P_{dpi} greater than 31 dBm, for F_{dpi} larger than 600 MHz.

Similarly, for the 5-stage CSVCO, the maximum susceptibility was also detected at F_{dpi} = 100 MHz as seen in Fig. 3 (b). This time, the minimum P_{dpi} equals 19 dBm, surpassing the power level of the 3-stage CSVCO. The reason for this behavior is currently under investigation. The deviation in the DC offset voltage (C3) had an effect on the failure for F_{dpi} higher than 700 MHz and when power levels reached 34 dBm. To sum up, the overall behaviors of the multi-stage CSVCOs were comparable, besides the fact that the 5-stage CSVCO had a greater immunity over the entire DPI frequency range.

Contrarily, for the 3-stage RO, seen in Fig. 4 (a), the failure at minimum power level was viewed at much higher F_{dpi} = 900 MHz & 950 MHz. Nevertheless, the DPI power levels were the same as the 3-stage CSVCO. The circuit was more immune to DPI at lower frequencies, failing at P_{dpi} = 31 dBm. The cause of failure at larger F_{dpi}, was due to the deviation in the output frequency (C1), while the V_{p-p} (C2) was stable. The reason for this behavior is because of the architecture of the RO. The C2 criterion was monitored before & after the output buffer and showed identical behavior. Also, since there are no biasing transistors in the RO, the RF signal is able to disturb the inverter directly, thus varying the output frequency. The supply voltage of the RO is very susceptible to EMI and thus can alter the output frequency substantially. The change in the DC offset voltage (C3) had an impact on the failure for F_{dpi} lower than 700 MHz and when power levels surpassed 31 dBm.

As shown in Fig. 4 (b), the failure at lowest power level, for the 5-stage RO, was noticed at F_{dpi} = 800 MHz, 850 MHz, 950 MHz & 1 GHz. The minimum P_{dpi} was the same as the 5-stage CSVCO, but exceeded the 3 stage RO. With the exception of the power levels, the performance of the multi-

P_{dpi} (dBm)	50	100	150	200	250	300	350	400	450	500	550	600	650	700	750	800	850	900	950	1000
37	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
34	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	F (C3)	FAIL	FAIL
31	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	F (C2)	F (C3)	FAIL	FAIL	F (C3)	FAIL	PASS	F (C2)	FAIL
28	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	F (C2)	F (C1)	FAIL	F (C1)	F (C1)	PASS	PASS	F (C2)	F (C2)	PASS	F (C2)	PASS	PASS	F (C2)
25	FAIL	FAIL	FAIL	FAIL	FAIL	F (C1)	PASS	PASS	F (C2)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
22	F (C2)	FAIL	F (C1)	F (C2)	F (C2)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
19	PASS	FAIL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
16	PASS	FAIL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
13	PASS	F (C2)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
10	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
7	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
4	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
1	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

F_{dpi} (MHz)

(a)

P_{dpi} (dBm)	50	100	150	200	250	300	350	400	450	500	550	600	650	700	750	800	850	900	950	1000
37	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
34	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	F (C2)	FAIL	F (C2)	FAIL	F (C3)	F (C2)	FAIL	F (C3)	F (C3)	F (C3)	F (C3)	F (C3)
31	FAIL	FAIL	FAIL	FAIL	FAIL	F (C2)	FAIL	F (C2)	FAIL	PASS	F (C1)	PASS	F (C1)	PASS	PASS	FAIL	PASS	PASS	PASS	PASS
28	FAIL	FAIL	FAIL	FAIL	F (C2)	PASS	F (C2)	PASS	F (C1)	PASS	PASS	PASS	PASS	PASS	PASS	F (C1)	PASS	PASS	PASS	PASS
25	F (C2)	FAIL	FAIL	F (C2)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
22	PASS	FAIL	F (C2)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
19	PASS	F (C2)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
16	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
13	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
10	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
7	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
4	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
1	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

F_{dpi} (MHz)

(b)

Figure 3. Susceptibility table of CSVCO: (a) 3 stage; (b) 5 stage.

P_{dpi} (dBm)	50	100	150	200	250	300	350	400	450	500	550	600	650	700	750	800	850	900	950	1000
37	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
34	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
31	F (C3)	F (C3)	F (C3)	F (C3)	FAIL	F (C3)	F (C2)	F (C2)	FAIL	FAIL	FAIL	FAIL	F (C3)	F (C3)	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
28	PASS	PASS	PASS	PASS	FAIL	PASS	PASS	PASS	FAIL	F (C1)	F (C1)	FAIL	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
25	PASS	PASS	PASS	PASS	F (C2)	PASS	PASS	PASS	F (C1)	PASS	PASS	FAIL	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
22	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	F (C1)	PASS	PASS	F (C1)	F (C1)	FAIL	FAIL	FAIL	FAIL
19	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	FAIL
16	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	F (C1)	FAIL	FAIL	F (C1)
13	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	F (C1)	F (C1)	PASS	PASS
10	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
7	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
4	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
1	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

F_{dpi} (MHz)

(a)

P_{dpi} (dBm)	50	100	150	200	250	300	350	400	450	500	550	600	650	700	750	800	850	900	950	1000
37	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
34	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	F (C3)	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
31	F (C3)	F (C3)	F (C3)	F (C2)	F (C2)	F (C2)	PASS	F (C1)	F (C2)	F (C3)	F (C2)	F (C2)	FAIL	FAIL	F (C3)	FAIL	FAIL	FAIL	FAIL	FAIL
28	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	F (C1)	F (C1)	PASS	FAIL	FAIL	FAIL	FAIL	FAIL
25	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
22	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	F (C1)	FAIL	FAIL	
19	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	F (C1)	F (C1)	PASS	F (C1)	F (C1)
16	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
13	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
10	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
7	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
4	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
1	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

F_{dpi} (MHz)

(b)

Figure 4. Susceptibility table of RO: (a) 3 stage; (b) 5 stage.

stage ROs was equivalent. Also, the deviation in the DC offset voltage (C3) had an influence on the failure at P_{dpi} greater than 31 dBm, for F_{dpi} less than 500 MHz.

To sum up, both CSVCOs & ROs showed different behaviour to DPI interference. The multi-stage CSVCOs were immune at higher F_{dpi} and were impacted by the deviation in output V_{p-p}, while the multi-stage ROs were immune at lower F_{dpi} and were affected by the unstability of the output frequency. For greater number of stages for both oscillators, the DPI immunity power levels were greater. The failure criterion of the DC offset was only reached for P_{dpi} greater than 31 dBm.

It can be seen that the frequency ranges of minimum immunity are identical in a given category regardless of the number of stages. However, the more stages, the lower the susceptibility of the oscillator. The studied CSVCOs are susceptible at much lower frequencies (around 100 MHz) than ROs (around 900 MHz). The main failure mechanism (lower incident power) for the CSVCO is the peak-to-peak output voltage, while it is the output frequency deviation for the RO. Moreover, the DC offset varied for higher frequencies for the multi-stage CSVCOs and for lower frequencies for the multi-stage ROs.

B. Supply Current & Output Power Comparison

Output power depends on the voltage and the total current monitored at the load. The primary motivation for reducing the power is increasing the lifetime of an oscillator and preserving the entire IC [14].

The nominal DC supply current, without DPI injection, was simulated as 3.51 mA (3-stage CSVCO), 2.62 mA (5-stage CSVCO), 505 μA (3-stage RO) and 1.15 mA (5-stage RO). That supply current was then monitored for two different power levels (27 dBm & 37 dBm) over the whole DPI frequency range. Only frequencies corresponding to maximum DC current were then considered. Those results are summarized in Table II.

It can be seen that the DC supply current increases significantly with RF injection power. Moreover, the maximum DC current is obtained when the injection frequency is close to the nominal operating frequency of the oscillators. Interestingly, the rise in DC current for an injection frequency (100 MHz) corresponding to the CSVCOs maximum susceptibility was smaller (4.5 mA for 3-stage and 7.7 mA for 5-stage), suggesting that a different mechanism is responsible for that increase. Further simulations are being carried out to investigate the operating points of the transistors. The ROs have a similar behavior except that their minimum immunity frequencies are closer to their nominal operating frequencies.

Furthermore, the output power for each oscillator (before the output buffer for ROs) was computed by multiplying the output voltage and current in time domain and integrating the result. It was observed that the frequency corresponding to maximum power was also found close to the nominal output frequency of each oscillator.

Table II
MULTI-STAGE OSCILLATORS OUTPUT POWER AND SUPPLY CURRENT

Type of Oscillator	Output Power ($P_{dpi} = 27$ dBm)	Output Power ($P_{dpi} = 37$ dBm)	Supply Current ($P_{dpi} = 27$ dBm)	Supply Current ($P_{dpi} = 37$ dBm)
3 Stage CSVCO Vin= 1.8V	1.03 mW ($F_{dpi} = 700$ MHz)	1.23 mW ($F_{dpi} = 700$ MHz)	11.5 mA ($F_{dpi} = 700$ MHz)	26.2 mA ($F_{dpi} = 700$ MHz)
3 Stage RO with buffer	1.44 mW ($F_{dpi} = 850$ MHz)	2.90 mW ($F_{dpi} = 850$ MHz)	16.1 mA ($F_{dpi} = 850$ MHz)	64.4 mA ($F_{dpi} = 850$ MHz)
5 Stage CSVCO Vin= 1.6V	759 µW ($F_{dpi} = 300$ MHz)	982 µW ($F_{dpi} = 300$ MHz)	9.6 mA ($F_{dpi} = 300$ MHz)	18.8 mA ($F_{dpi} = 300$ MHz)
5 Stage RO with buffer	1.15 mW ($F_{dpi} = 800$ MHz)	1.89 mW ($F_{dpi} = 800$ MHz)	14.7 mA ($F_{dpi} = 800$ MHz)	46.5 mA ($F_{dpi} = 800$ MHz)

IV. CONCLUSION & OUTLOOK

In view of preventing costly re-design after manufacturing, IC immunity must be predicted early in the design stage. This paper compares, through simulation, the immunity at IC level of multi-stage CSVCOs & ROs, when exposed to DPI. The failure criteria considered were output frequency, peak-to-peak output voltage and DC offset output voltage. The multi-stage CSVCOs were susceptible to DPI at lower frequencies (around 100 MHz), while the multi-stage ROs were susceptible at higher frequencies (around 900 MHz). All oscillators showed a greater (by 6 dBm incident power) DPI immunity when the number of inverter stages increased. Moreover, the DC supply current & output power surged for all circuits when the RF injection power levels were raised. The maximum power and current were detected for an injection frequency close to the nominal oscillating frequency of each oscillator.

As an outlook, the properties of the multi-stage CSVCO & RO will be further examined and compared to simulations, after the PETER_ESEO IC is fabricated and tested for conducted immunity measurements. It will also be investigated how the temperature and relative humidity may influence the immunity of each oscillator.

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