# A Comparative Study of On-Chip CMOS S&H Voltage Sensors for Power Integrity: SOI vs. Bulk

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***Abstract*—This paper evaluates the performance of two on-chip sample & hold (S&H) voltage sensors, usable for power integrity measurements, with the aim to compare silicon-on-insulator (SOI) & bulk CMOS technologies. Both sensors were designed and simulated in 180 nm 5 V AMS-bulk and XFAB-SOI processes, using optimized parameters and compatible devices. The fundamental variables analyzed were power consumption, leakage current, slew rate (SR), and transient output voltage, under process, voltage and temperature variations. Compared to bulk technology, SOI was found to have lower power consumption (by 2.2 mW in average) and leakage supply current (by 9.5 pA at 27°C), higher sensitivity to process variations (up to 88% additional slew rate versus 39% at 80°C), higher resilience to temperature changes (6% in output voltage), and a larger occupied area. The SOI sensor is intended to be fabricated and used to evaluate injected continuous wave and transient disturbances as well as voltage fluctuations due to internal activity on power distribution networks.**

***Index Terms*—Integrated circuits, voltage sensor, SOI, PVT, power integrity**

## I. Introduction

In standard industries, bulk CMOS is a very mature technology having high performance and lower manufacturing costs. However, increasing integration degree and signal transmission rates highlight some challenging aspects. The most promising technology to overcome those limitations is the silicon-on-insulator (SOI) CMOS process [1].

SOI employs a thin layer of silicon, eliminating most of the parasitic capacitances found in bulk CMOS [2]. Integrated circuits (IC) designed with SOI technology have several vital advantages: faster performance, lower power dissipation, low leakage effect, and high integration [3]. SOI has also demonstrated its potential for radio frequency (RF) applications [4].

Generally, ICs can produce and/or be subject to RF disturbances, which are evaluated at low frequencies that most of them tend to radiate [5]. An on-chip voltage sensor based on deep-downsampling has already been proposed to characterize these coupled disturbances [6]. It measures induced internal voltage fluctuations, determining actual sensitivity to electromagnetic interference (EMI) [7]–[9]. However, such sensors have not been implemented in SOI technology, benefiting from reduced substrate losses and withstanding harsh environments (high temperature, radiations) [10].

A robust on-chip sample & hold (S&H) voltage sensor was designed and simulated in both 5 V 180 nm XFAB-SOI and AMS-bulk technologies in the current study. Process, supply voltage, temperature (PVT) variation tests were carried out on both sensors to compare their performance. These tests represent an integral part of modern chip design flows and accurately characterize a circuit's worst-case behavior [11]. Transient analysis runs were executed at extreme corners, and essential electrical parameters: power consumption, leakage current, and output voltage were analyzed. Consequently, this paper aims to demonstrate that a voltage sensor designed with equivalent specifications can function better in SOI compared to bulk technology when exposed to critical conditions.

The objective of selecting the S&H on-chip voltage sensor is that it will be integrated into a test chip, in order to precisely quantify RF disturbances with IC ageing and help develop EM immunity & emission behavioral models.

The paper is organized as follows. Section II describes the design procedure of the sensors and the simulation setup configurations. Section III focuses on the extensive analysis of the simulation results, while concluding contributions of this study are presented in Section IV.

## II. Materials and Methods

This section introduces the voltage sensor's principle of operation followed by the design of its amplifier with the associated current source. All circuits were designed using Cadence Virtuoso, and the simulations were obtained in Spectre. Two identical sensors were simulated in SOI and bulk CMOS 5 V using 180 nm technology kits, provided by XFAB and AMS foundries, respectively. The sensors are designed to have similar characteristics and matching size dimensions. The SOI version is planned to be manufactured into a 1.52 × 1.52 mm mini-Asic test chip in XFAB 180 nm 5 V technology.

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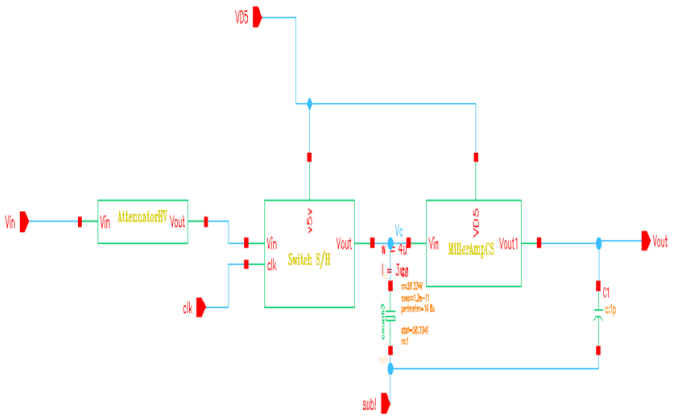



Fig. 1. Schematic of the S&H voltage sensor.

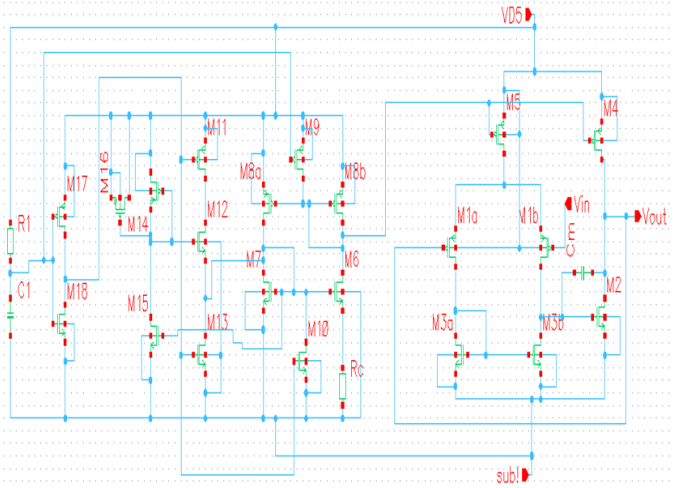



Fig. 2. Transistor level schematic of the Miller amplifier with current source & start-up circuit.

### A. S&H Voltage Sensor Description

The CMOS voltage sensor is made up of the following elements (Fig. 1 from input to output):

- a resistive attenuator, which downscales the input voltage within 0 to 5 V voltage range,
- a sampler cell composed of a storage capacitor, a 5 V CMOS pass gate driven by an external clock, with a 1 GHz bandwidth,
- a unity gain differential Miller amplifier (5 V supply), with a 100 MHz bandwidth to ensure a reliable transient response, including a current source with a start-up circuit.

The voltage sensor's fundamental principle is based on intentional aliasing, operating in subsampling conditions well below the Nyquist criteria, enabling transpose of high-frequency signals (1 GHz in this case) down to a few MHz. Copies of the input signal spectrum are created around each multiple of the clock frequency. In our case, a 0.9999 MHz sampling frequency would transform a 1 GHz input sinewave signal into a 100 kHz one. We can exclude the influence of parasitic elements caused by the package, bonding, and PCB trace at such a low frequency. The signal amplitude observed at the output behaves as a linear function of the input signal amplitude. Note that this sensor can also be used in random sampling mode for non-sinusoidal signals.

The first stage is the input attenuator, a resistive divider with an attenuation ratio fixed at 1/10 to measure any voltage ranging from 0 to 50 V. Compensation capacitors were added to include the effect of the resistors' parasitic capacitance and the load of the sampler stage. These capacitors were appropriately sized to keep the high-frequency response flat. Metal-Insulator-Metal (MIM) capacitors are used for both technologies since they have high breakdown voltages and can withstand more than 50 V.

As detailed in [12], the second stage is the sampler cell, which includes a switch and a holding capacitor. It is designed to have a 1 GHz bandwidth. To maintain this bandwidth, the switch's on-state resistance is reduced by increasing the MOSFETs' widths and keeping the holding capacitor value as minimum as possible. In XFAB and AMS design kits, the minimum capacitor values are limited to 11 fF and 30 fF, respectively. Therefore, the latter was selected for a fair comparison. To ensure an almost constant resistance in the whole voltage range, the PMOS is five times wider than the NMOS. Dummy transistors were added to the switch to compensate for parasitic capacitances.

The output stage is a differential, 5 V supply, Miller amplifier with unity gain up to 100 MHz. Its primary function is to provide isolation of the sensor from all noise sources to ensure accurate measurements. The Miller amplifier was designed to keep the gain constant, improve bandwidth, decrease output impedance, and mitigate stability problems. The 1 pF load capacitance at the output of the amplifier represents the capacitance of the output pad of the die (Fig. 1). The comprehensive design of the Miller amplifier and its current source is explained in the following subsection.

### B. Design of Miller Amplifier with Current Source

The designed unity gain Miller amplifier consists of three blocks: differential amplifier, common source amplifier, and the current source with a start-up circuit, as demonstrated in Fig. 2. The common source amplifier ensures a maximum output swing, and a Miller capacitor (Cm) connects it to the differential circuit [13], aiming to stabilize the circuit by improving the phase margin. In order to minimize the chip area, the current source provides a small reference current, which is replicated by duplicating the unit transistor M8b of the current source as many times as needed in transistors M4 and M5 to obtain the desired currents in the amplifier with proper matching (Table I). A start-up circuit (M9 to M18, R1 and C1) is added to ensure that the current source reaches a non-zero quiescent operating point when the power supply is turned on.

The Miller amplifier's aspect ratios (W/L) were optimized using Jespers's and Murmann's sizing methodology [14] using pre-computed SPICE generated look-up tables and specific

TABLE I
MILLER AMPLIFIER CHARACTERISTICS

| Miller amplifier parameters | XFAB-SOI | AMS-bulk |
|---|---|---|
| W1 / L1 (µm) | 70.6 / 0.6 | 59.2 / 0.7 |
| W2 / L2 (µm) | 125.2 / 0.5 | 110.8 / 0.7 |
| W3 / L3 (µm) | 25.3 / 0.6 | 16.2 / 0.7 |
| W4 / L4 (µm) | 483.1 / 1.0 | 357.2 / 1.0 |
| W5 / L5 (µm) | 115.9 / 1.0 | 89.3 / 1.0 |
| W6 / L6 (µm) | 30.0 / 1.0 | 25.0 / 1.0 |
| W7 / L7 (µm) | 8.34 / 1.0 | 6.3 / 1.0 |
| W8 / L8 (µm) | 4.83 / 1.0 | 3.57 / 1.0 |
| Miller capacitance, $C_m$ (pF) | 1.90 | 1.33 |
| Biasing current, $I_4$ (mA) | 1.56 | 1.10 |
| Biasing current, $I_5$ (µA) | 390 | 275 |
| Limiting resistor, $R_c$ (kΩ) | 6.07 | 9.12 |
| Bandwidth, BW (MHz) | 111.7 | 121.3 |
| Phase margin, PM (deg) | 76.6 | 74.3 |
| Slew rate, SR (V/µs) | 83.4 | 90.8 |

Matlab functions. It makes it possible to quantify trade-offs among transconductance efficiency, power consumption, gain, and area. Table I shows the unity gain Miller amplifier specifications for both technologies. The W/L ratios of the SOI are larger than bulk due to its MOSFETs' having higher transconductance, more current, lower parasitic junction capacitance, and higher gate oxide thickness. The bandwidth (BW) and slew rate (SR) of the bulk amplifier are slightly larger than SOI, but having a lower phase margin. The biasing current of the SOI is higher than bulk.

## III. SIMULATION RESULTS AND DISCUSSION

This section presents all transient, AC, PVT, and parametric simulations related to the voltage sensor in 5 V 180 nm XFAB-SOI and AMS-bulk. All transient simulations were timed to 10 $\mu$s since it represents the single 100 kHz aliased output wave. All AC simulations have a frequency range of 10 GHz, in a logarithmic scale, with a 25 V DC offset at the attenuator input. While the nominal temperature is 27 °C, the temperature and voltage ranges for PVT simulations are (−40 °C to 80 °C in 5 °C steps) and (4.4 V to 5.6 V in 0.1 V steps), respectively, as indicated by the foundries. For process variations, only extreme corners, worst power (WP), and worst speed (WS) are considered.

### A. PVT Corner Analysis

PVT variations can increasingly affect the sensitivity of the CMOS circuit performance. A significant number of possible corners are applied to examine circuit timing. The process variation accounts for deviations in the semiconductor fabrication process. Standardly, it is reviewed as a percentage change in the performance calculation. Considerable variations in its specifications can be oxide thicknesses, impurity concentration densities, and diffusion depths. These adversely affect the sheet resistance, threshold voltage, and aspect ratios of CMOS transistors [15].

TABLE II
SLEW RATE (SR) VS. PVT CORNERS

| PVT Corners ($V_{DD}$ = 5V) | SOI (SR,V/µs) | bulk (SR,V/µs) |
|---|---|---|
| C0 (WP, T = -40°C) | 85.8 | 94.9 |
| C1 (WP, T = 80°C) | 150.1 | 119.3 |
| C2 (WS, T = -40°C) | 52.1 | 66.7 |
| C3 (WS, T = 80°C) | 79.9 | 85.6 |

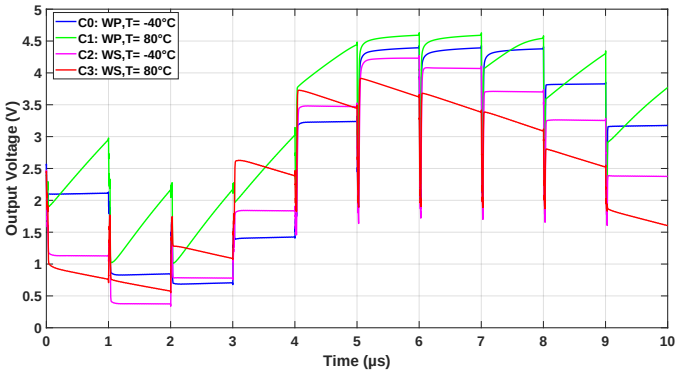
During standard operation the supply voltage can typically vary from the nominal value. The saturation current and the delay of a cell are dependant on the power supply. When the power is unconstant in a chip, each cell operates quicker with rising supply voltage, consequently reducing the delay. All circuits, have temperature variations, because of the power consumption linked to the switching of the CMOS transistors. Excessive temperatures will reduce the mobility of the transistors resulting in an increased propagation delay. However, the temperature surge also decreases the threshold voltage and leads to higher current and accelerated performance. Hence, the equivalent change produces adverse effects that will highly depend on the circuit's supply voltage. For bulk CMOS circuits, the robustest performance is reached at the rapid process (worst power), high supply voltage, and reduced temperature [16]. Therefore, a PVT corner analysis was performed on both S&H voltage sensors in SOI and bulk CMOS technologies to compare the effects.

A 4-corner transient SR simulation was performed on each Miller amplifier with extreme temperature and process variations while keeping the supply voltage constant at 5 V. The amplifier in each technology is operated by a dedicated 5 V power supply, separated and isolated from the circuit's other power supplies. Thus, we are only monitoring the effects of process and temperature in this case. The results are displayed in Table II.

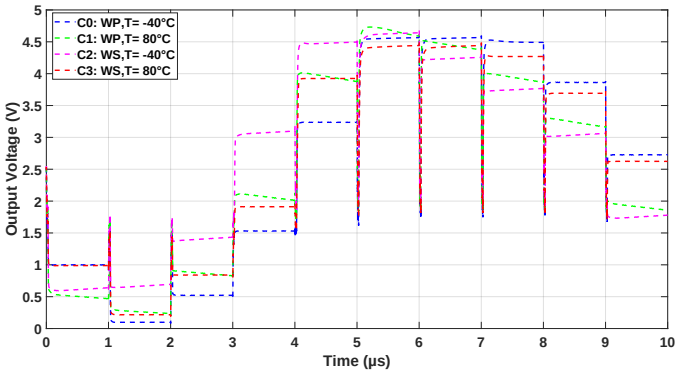
The SR of each Miller amplifier, at corners C1 and C2, is at its maximum and minimum, respectively, for both technologies (Table II). This result is due to the slew rate being directly related to both process and temperature. A faster process results in quicker switching of the transistors, and higher temperature increases the current coming from the differential pair. Moreover, it can be noticed that the SR of SOI amplifier is more sensitive to either process or temperature. Comparatively, the SR of both amplifiers was either increased or decreased slightly on corners C0 and C3, respectively, with the effects of process and temperature competing against each other.

Transient simulations on the same corners were implemented for the output voltage of each S&H voltage sensor. The peak-to-peak output voltages ($V_{p-p}$) of the sensor, in bulk and SOI CMOS technologies, at nominal conditions are 4.4 V and 3.8 V, respectively. The latter was not expected, since the output swing is related to the transconductance efficiencies (gm/Id) of the output transistors [14], which are the same in both designs.

The $V_{p-p}$ and waveform remain unchanged at corner C0 for

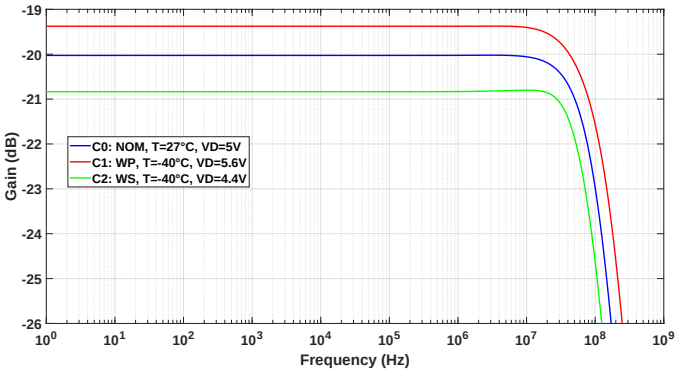



(a)

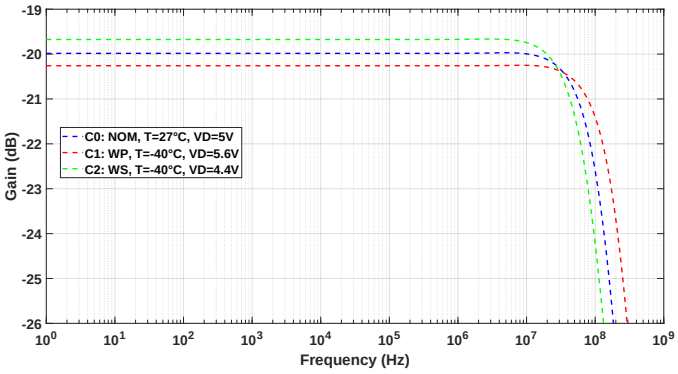



(b)

Fig. 3. Transient PVT simulation ($V_{DD}$ = 5 V) of output voltage: (a) SOI; (b) bulk.




(a)




(b)

Fig. 4. AC PVT simulation of gain response: (a) SOI; (b) bulk.

both technologies. Corner C1 displayed different responses for both technologies. For SOI, the $V_{p-p}$ reduces by 0.2 V, and the SR of the output voltage signal changes abruptly. The curve is deformed at the falling end. This could be due to the process variation in the holding capacitor or the switches (the same behavior being observed at the amplifier input node). For bulk, $V_{p-p}$ reduces by 0.1 V, and the SR of the output signal slightly falls at the rising end.

At corner C2, SOI $V_{p-p}$ remains the same, only the curve faces a negative offset of 0.2 V, and the waveform remains unchanged. For bulk, $V_{p-p}$ reduces by 0.4 V and the curve has a positive offset of 0.2 V. At corner C3, the overall $V_{p-p}$ of SOI and bulk are reduced by 0.4 V and 0.2 V, respectively. For SOI, the effect is more severe as the overall SR of output signal reduces and the output voltage graph is deformed at the rising end. This could be due to the holding capacitor discharging slowly while, for bulk, the output SR and waveform remains unaltered.

To sum up, both technologies' best transient response is observed when the temperature is low, and the process is fast. Contrarily, the worst output response (lowest $V_{p-p}$ and highest offset) for bulk is at corner C2, which means that the threshold voltages of the MOSFETs significantly increase with a slower process. Also, at this corner, Miller amplifier in AMS technology had the minimum SR, which is related to $V_{p-p}$; however, the latter had no effect on the waveform shape. For SOI, the worst output response was observed at both C1 and C3 corners. Since the SR of the output was reduced at both corners, as was $V_{p-p}$. As described earlier, the waveform of the output signal is affected more by the holding capacitor charging speed, the amplifier's SR had little effect on the output voltage signal. This uncertainty remains to be clarified, by studying the influence of process and temperature variations on the overall SOI S&H voltage sensor.

A 64-corner PVT AC simulation was performed on both sensors, and the corners resulting in the largest divergence from nominal values were plotted in Fig.4. The gain of the sensors was −20 dB due to the 1/10 attenuator. The bandwidth of SOI and bulk CMOS voltage sensors at nominal conditions is 100.5 MHz and 110 MHz, respectively. Including process and temperature, the supply voltage was varied from 4.4 V to 5.6 V, which are the maximum limits of the MOSFETs used in both technologies.

The two extreme corners were observed at the constant lowest temperature (−40 °C): the extreme process (WP, WS) and supply voltages (4.4 V, 5.6 V). However, the behavior of SOI and bulk was quite different. At corner C1 (fast process, high voltage), the SOI sensor's bandwidth and gain were increased to 200 MHz and −19.3 dB, respectively. Moreover, for bulk, the bandwidth was increased to 180 MHz, but the gain dropped to −20.4 dB. At corner C2 (slow process, low voltage), the SOI sensor's bandwidth was lowered to 80 MHz, and its gain reduced to −20.8 dB. Furthermore,

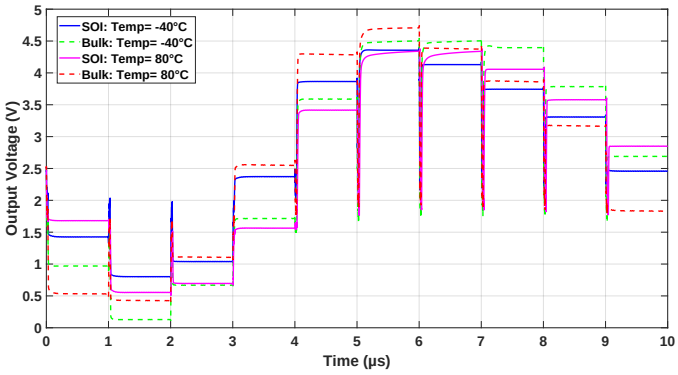



Fig. 5. SOI vs. bulk: output voltage as a function of temperature.

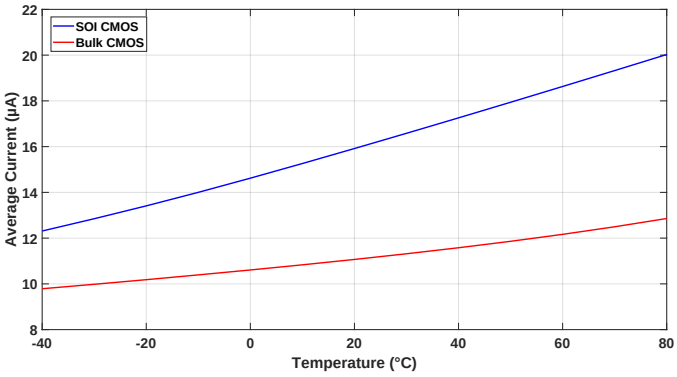



Fig. 6. SOI vs. bulk: source average current as a function of temperature.

the bulk sensor's bandwidth was reduced to 85 MHz but its gain increased to −19.6 dB. To summarize, at higher supply voltages and faster processes, the bandwidth of both sensors was increased. This is due to an increase in the DC operating current of the amplifier stages, which is even more significant for SOI. At the same corner, the gain of the SOI sensor was increased, while it was reduced for bulk. The reason could be due to variations in the attenuator, the amplifier itself being put in a unity gain closed loop.

### *B. Temperature Effect*

This section demonstrates the effect of temperature only on the voltage sensor's essential parameters: output voltage, average current from the current source and the leakage current from the supply when the circuit is powered off.

After a parametric simulation of the output voltage with a temperature change, the extreme corners were plotted in Fig. 5. In bulk technology, there was a 0.25 V rise in the offset voltage with an increase in temperature, but the $V_{p-p}$ value remained constant. Contrarily, for SOI, there was hardly any rise in the offset voltage with a temperature change, but the $V_{p-p}$ value was increased by 0.2 V. This transient analysis shows the SOI sensor provides a more robust result at elevated temperatures, as expected. This result further explains the previous effects on waveforms caused by process variations, not by temperature, for SOI technology, since the waveform is not altered. To sum up, SOI seems to be very sensitive to process variations.

The Miller amplifier's current source generates 15.6 $\mu$A and 11 $\mu$A in SOI and bulk, respectively, at room temperature. Both currents were proportional to temperature change. The rate of current change with temperature for SOI (62.5 nA/°C) was higher compared to that of bulk (29.1 nA/°C), as observed in Fig. 6. One reason for that behavior is the steeper reduction of the threshold voltages of SOI MOSFETs with temperature compared to bulk, resulting in higher current and faster performance.

As far as the leakage current is concerned, at the nominal temperature, a higher current was monitored in bulk (12.4 pA) compared to SOI (2.88 pA) S&H sensors, as expected. One interesting observation was the exponential increase of the leakage current for bulk compared to SOI with rise in temperature; e.g. at 80°C, the amount of leakage current was 80 pA and 3.8 pA in bulk and SOI sensors, respectively.

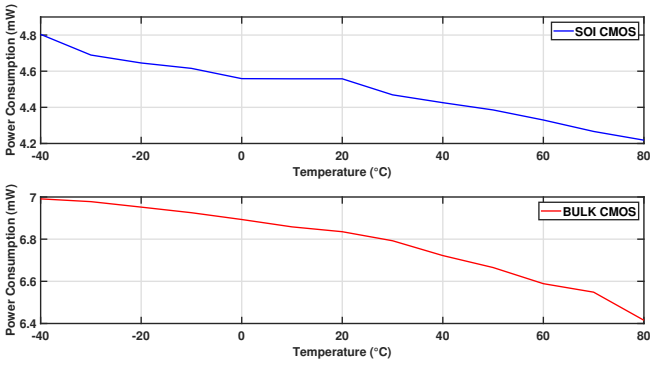



Fig. 7. SOI vs. bulk: power consumption as a function of temperature.

### *C. Power Consumption*

SOI technology lowers the junction capacitances and allows the circuits to work at a more reduced power maintaining identical speeds [17]. Lower power consumption seems to be the most distinguished advantage SOI has over bulk. The power consumption of the sensors was evaluated at the output node of the 1 pF load capacitance (Fig. 1). Power (4.5 mW) was lower in SOI technology than in bulk (6.8 mW), even though output impedances were the same. Fig.7 shows the variation of power consumption as a function of temperature. It can be seen that power is inversely proportional to temperature, showing a gradual reduction of 0.6 mW in the considered temperature range for both technologies. However, for SOI, power consumption remains constant between 0 and 20 °C. The decrease in power consumption with temperature is linked to reducing mobility in MOSFETs, hence their drain current.

## IV. Conclusion & Perspective

With the aim to compare SOI and bulk processes, this paper investigates a S&H voltage sensor, usable for power integrity measurements, when subjected to process, voltage and temperature variations. Compared to bulk technology, the SOI on-chip sensor has lower power consumption (by 2.2 mW

in average) and leakage supply current (by 9.5 pA at 27°C), higher sensitivity to process variations (up to 88% additional slew rate versus 39% at 80°C), higher resilience to temperature changes (6% in output voltage), and a larger occupied area. That makes SOI a promising approach to build a more resilient on-chip S&H sensor.

As a perspective, SOI characteristics will be further explored after fabricating the on-chip sensor, mounting it on a PCB board, and testing it for RF EMI immunity & emission measurements. More specifically, injected continuous wave and transient disturbances will be evaluated on a prototyped chip as well as voltage drops caused by internal activity on power supply rails. The reliability and ageing aspect of SOI will also be investigated. This study covers the first step to developing predictive EM behavioural IC immunity & emission models in SOI, including thermal stress and ageing.

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