Digital and Analogue Hardware Design of an On-Board EMI Detector

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***Abstract*—The conceptual design of an EMI detector based on a pair of transmission lines sending inverted data has been presented previously. This paper focuses on the actual hardware design of such an EMI detector. The prototype of the EMI detector is implemented using both analogue and digital hardware designs. In the analogue design, the EMI detector detects the presence by processing the signal at the receiver end directly using analogue electronic components. In the digital design, the EMI detector uses an analogue to digital converter (ADC) to convert the voltage signal from the receiver end into its digital form. This voltage is further processed using a Field Programmable Gate Array (FPGA), which generates a warning when EMI is present. This paper compares the operation and performance of both designs of the EMI detector in a harsh electromagnetic (EM) environment.**

***Index Terms*—EMI, EMC, Functional Safety, Risk Management, Detection**

I. Introduction

The advent of autonomous systems, Industry 4.0 and the Internet of Things (IoTs) have significantly increased the demand for sophisticated and dependable electronic systems in recent years. More and more mission- and safety-critical devices are used in our daily lives. At the same time, due to the growing usage of wireless communication and high-power switching devices, the electromagnetic (EM) environment is getting harsher and more polluted every day. EM disturbances can interfere with electronic data, affect performance, and in extreme cases, cause fatal errors. Because of the above, the combination of the disciplines of electromagnetic compatibility (EMC) engineering and system safety engineering are gaining huge importance.

The recently published standard IEEE 1848, focuses on techniques and measures (T&Ms) to enhance the safety of a system by properly managing functional safety and other risks regarding EM disturbances [1]. These T&Ms aim to prevent errors, malfunctions or failures in signal, data and power supplies. The main goal of these T&Ms is to minimize the actual impact of EM disturbances. In the presence of EM disturbances, the system should preferably keep working as foreseen, or if that is deemed to be not sufficiently safe, continue with limited performance or, in the extreme case, shut down temporarily to avoid fatal errors (safe-state).

The actual implementation of communication channels plays a vital role in the safe transmission of data. EM disturbances in a wired communication channel are one of the major concerns for functional safety engineers. The EM disturbance can affect the communication channel, leading to the corruption of transmitted data. Therefore, many software and hardware-based T&Ms are designed for dealing with possible interference on the data in a communication channel [2]. Software-based techniques include Error Correction Codes (ECC) and Error Detection Codes (EDCs), which aim to detect and correct data affected by EM disturbances [3], [4]. Hardware-based techniques focus on diversity redundancy, for example, by spatial [5], frequency [6], and time diversity [7]. Unfortunately, the available T&Ms are not able to ensure correct transmission of data or detect corrupt data in the presence of EMI in all cases.

As an additional T&M, an on-board EMI detector based on a pair of transmission lines sending inverted data has been proposed in [8], [9]. The EMI detector generates a warning when it detects EMI disturbances in the data on the transmission lines. This warning can help the system to follow a precautionary procedure by retransmitting the data or, in the extreme case, by shifting the system to reduced performance or a safe-state. The EMI detector was tested by software-based simulations using continuous-wave disturbances and a Monte-Carlo based simulation-framework [8], [9]. The continuous wave simulations use a sinusoidal EMD induced voltage as an EM disturbance to analyze the performance of the EMI detector. In these simulations, amplitude, frequency, incoming phase, and phase difference between data transmission lines of EMD induced voltage is varied for the analysis. The Monte-Carlo based simulation framework uses an EM wave in a simulated reverberation room like environment. Therefore, the induced voltage in the Monte-Carlo based simulation framework depends upon the magnitude, direction, and polarization of the incident plane waves. The EMI detector was able to detect EMI induced bit errors in most cases except when the EMD frequency is a multiple of the sampling rate [8].

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In this paper, analogue and digital hardware designs of the EMI detector are presented with the aim to practically and physically analyze their performance. In the analogue design, the EMI detector processes the signal received from the data transmission lines directly using analogue electronic components. In the digital design, the voltage in both data transmission lines is converted to digital signals using an ADC. These digital signals are further processed using a Field Programmable Gate Array (FPGA). In both designs, the EMI detector aims to generate a warning when EMD is interfering with the data.

The remainder of this paper is organized as follows: Section II discusses the theoretical work behind the hardware design of the EMI detector. Section II-A describes the analogue design of the EMI detector. Section II-B elaborates the details of the digital design of the EMI Detector. Section III evaluates the design of the EMI detector. Section IV deduces the results from the analysis. Lastly, Section V provides concluding remarks.

II. Hardware design

In the development of the hardware design of the EMI detector, differential data transmission lines are used. The designed EMI detector receives a signal from the receiver end of both data transmission lines to detect EMI disturbances. This signal is processed by performing the analytical operations as proposed in [8], [9], including the addition and subtraction of the received signal. The aim of these operations is to analyze the EMI-induced voltage correctly. The EMI detector generates a warning when the induced voltage is higher than the predetermined threshold voltage. Fig. 1 shows the block diagram of the designed EMI detector. For more details about the theoretical concepts behind the EMI detector, the reader is referred to [8].

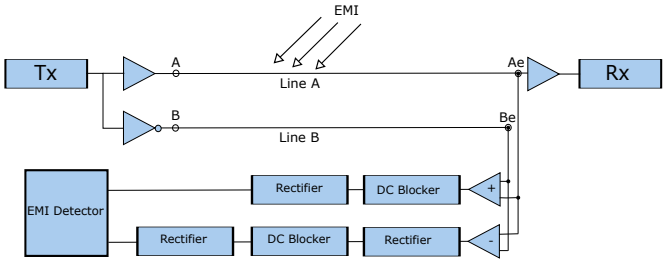

Fig. 1. EMI Detector Block Diagram

A. Analogue Design

In the analogue design of the EMI detector, the EMI detector processes the signals directly using analogue electronic components. The theoretical results in [8], [9] show that the EMI detector may not detect bit errors when the frequency ratio is an integer multiple of the sampling rate. The frequency ratio is defined as the ratio of the EMI frequency to the bit frequency. The design of the EMI detector focuses on a bit frequency of 100MHz. In order to verify the shortcomings identified in the theoretical design, all electronic components selected for the EMI detector work for at least a frequency of 300MHz, i.e. three times the selected bit frequency. The analogue design uses an OPA 699ID for all operational amplifiers. The OPA 699ID is a wideband, high-frequency amplifier with a gain-bandwidth product of 1GHz. In this design, the data transmission lines use Low Voltage Differential Signalling 2.5V (LVDS2.5). LVDS2.5 uses a 2.5V supply and 1.25V common-mode. To differentiate the logic ”high” and ”low” of the transmitted data, LVDS2.5 needs at least a differential swing of 350mV. The important components of the EMI detector are implemented as follows.

1) Adder: The adder adds up the voltages received from both data transmission lines. The adder is implemented by using non-inverting operational amplifiers. The addition of the voltages from both data transmission lines leads in ideal situations to a constant DC output voltage. This constant voltage is removed afterwards by a DC blocker based on a differential amplifier. This differential amplifier is fed by an external voltage supply.

2) Subtractor: The subtractor subtracts the voltages received from both data transmission lines. It is implemented by using a simple differential amplifier. The gain of the amplifier is more than one to amplify the difference of EMD induced voltage between data transmission lines. Therefore, the subtractor both subtracts and amplifies the voltage.

3) Rectifier: In order to rectify the signal, a full-wave rectifier is designed. There are two options for building a rectifier: by using diodes or MOSFETs. The voltage drop of diodes can diminish the induced voltage, whereas, high-frequency MOSFETs with lower threshold voltage are not commercially available discretely. Due to this, a diode-based rectifier followed by an operational amplifier is used. The operational amplifier reduces the impact of the voltage drop over the diodes and allows the EMI detector to analyze EMI disturbances with adequate sensitivity.

4) Voltage Buffer: Voltage buffers are commonly used to increase the input impedance. These ensure that there is no voltage drop by subsequent components. The voltage buffer is based on a simple operational amplifier.

5) Comparator: The comparator is a crucial component of the EMI detector, as it generates a warning if the EMI induced voltage is higher than the threshold voltage. Prior to this last step, the EMI detector performs separate addition and subtraction of the signal received from the data transmission lines followed by rectification and the removal of the DC component. Signals from the adder and subtractor are separately fed to two comparators. The comparator is also designed using OPA699ID. The value of the threshold voltage of comparators can be set using an external voltage supply.

B. Digital Design

In the digital design of the EMI detector, an ADC converts the received voltage from the data transmission lines to digital signals. An FPGA is used to process the signal and generate a warning. In addition, the digital design helps to analyse signals at each step and determine the impact of each block on

the performance of the EMI detector. Fig. 2 shows the block diagram of the digital design of the EMI detector. The main components of the digital design are as follows.

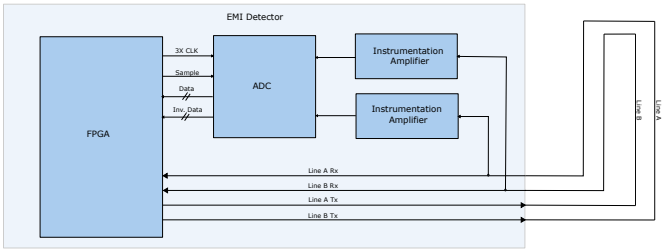

Fig. 2. Block Diagram of Digital Design of the EMI Detector

1) FPGA: The FPGA is the main processing unit in the digital design of the EMI detector. The main job of the FPGA is to transmit and receive data and also to perform signal processing, including addition, subtraction, rectification, and removal of the DC voltage. The FPGA transmits and receives data in a binary form. It generates a warning and records the data that can be used for further analysis. The FPGA also ensures retransmission of data in case of a warning. In this design, a Spartan-6, XC6SLX4(Xilinx) was used, with a TQFP144 package for the ease of soldering.

2) Analogue to Digital Converter (ADC): The digital design of the EMI detector uses a MAX105ECS ADC to convert the received analogue voltage to a binary representation of the voltages. The MAX105ECS is a 6-bit dual-channel, fully-differential ADC with 800 mega-samples per second (MSPS) sampling rate and +5V/-5V power supplies. Unfortunately, this ADC can only work within limited differential and common-mode input voltage ranges. This ADC can detect a differential voltage swing of 400mV from 1V to 1.4V. The received voltage from the data transmission lines is shifted to the receivable voltage range of the ADC. This is done by a set of operational amplifiers which attenuate and shift the voltage. Instrumentation amplifiers with high input resistance are used to feed the ADC. A high input impedance will ensure there is no voltage drop because of external connections of the EMI detector. Overall, the above settings ensure that the ADC can work effectively for EMI induced voltages from -5V to +5V.

3) Voltage Sources: There are four voltage sources for different components present in the digital design of the EMI detector. The primary USB connection supplies 5V input voltage, which is further converted according to the particular requirements. Linear and switch-mode regulators are used to generate the required voltages. In the design, voltage supplies of 1.2V, 2.5V, 3.3V, 5V and -5V are used.

4) Programmable Read-Only Memory (PROM): The job of the PROM is to save and provide the configurations for the FPGA. It can be programmed by using a JTAG connection. In this design, the XCF04 PROM model is used, it contains 4MB of memory.

III. Overview of Designs

The schematics and PCB designs of the EMI detector are described in this section. Fig. 3 shows the analogue design of the EMI detector. The module on top of the schematics shows an adder followed by a DC blocker and rectifier. The module in the middle shows the subtractor followed by a rectifier, DC blocker and another rectifier. The comparator is used at the end of the EMI detector to generate a warning if the EMI induced voltage is higher than the threshold voltage. The module at the bottom shows the decoupling capacitance of the EMI detector.

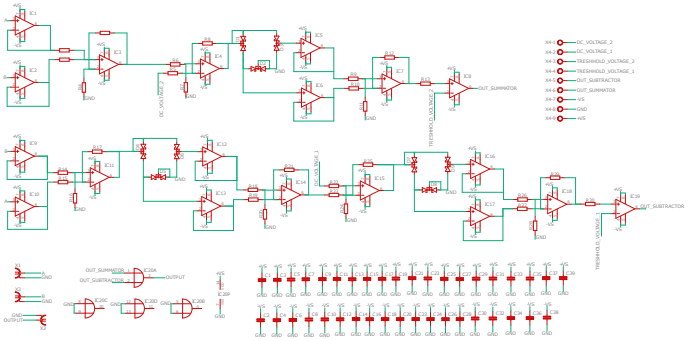

Fig. 3. Analogue EMI Detector Schematic

The schematics of the digital design of the EMI detector is shown in Fig. 4. In the schematics, the FPGA is present at the rightmost corner. Voltage regulators are arranged on the top left side of the schematic, and capacitors at the bottom left. Operational amplifiers to convert the voltage to the required range of ADC are shown on the top. The ADC, PROM, clock and set up for the USB connection are shown in the middle of the schematic design.

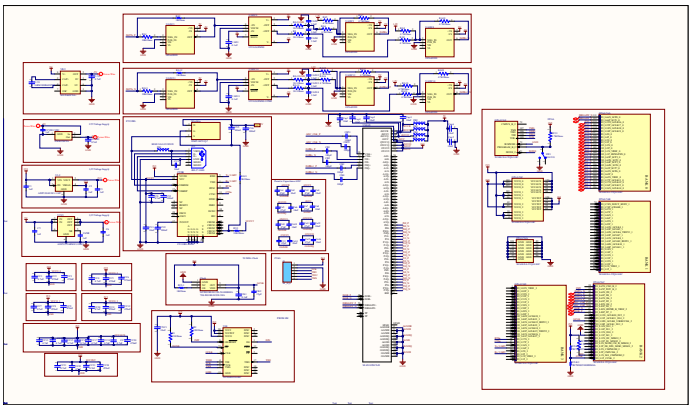

Fig. 4. Digital EMI Detector Schematic

The PCB of the analogue design consists of four layers: layer 1 for signal traces and components, layer 3 for power traces, and layers 2 and 4 for ground planes. The voltage sources and data transmission lines are externally connected with the PCB design using SMA connectors. Fig. 5 shows the PCB design of the analogue design of the EMI detector.

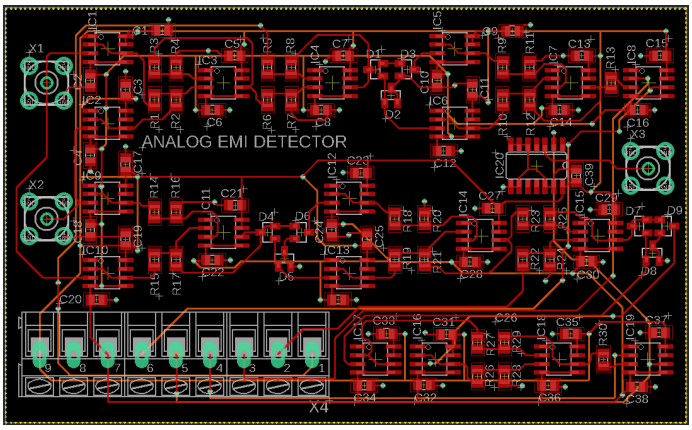

Fig. 5. PCB Layout of the Analogue EMI Detector

The digital design of the EMI detector contains all components, voltage sources, data transmission lines needed for the operation of the EMI detector on a single PCB. The PCB design consists of six layers: layers 1 and 3 for signal traces, layer 2 and 4 for ground layers, layer 5 for power traces, and layer 6 for data transmission lines. This PCB is compliant with the IEC 61967-2 and IEC 62132-2 standards. The PCB layout of the digital design of the EMI detector is shown in Fig. 6.

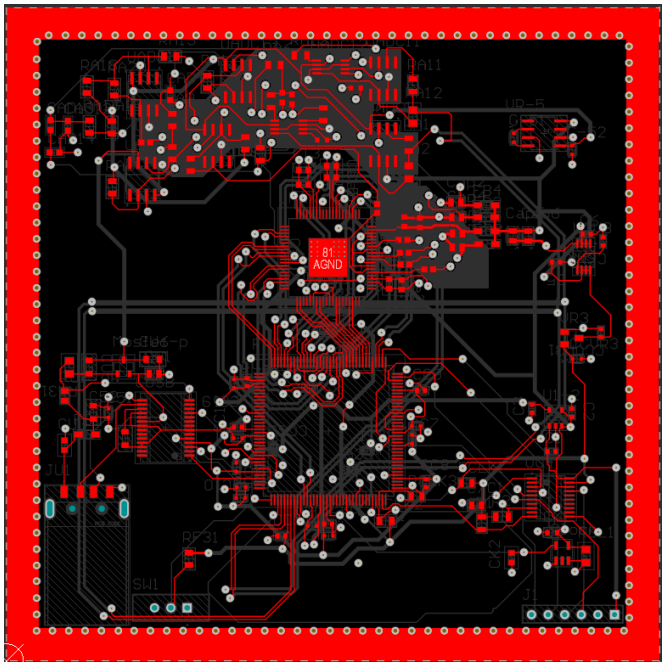

Fig. 6. PCB Layout of Digital EMI Detector

The PCB design of the analogue EMI detector has been fabricated and is shown in Fig. 7. Unfortunately, because of COVID related delays, a few components of the digital design were not delivered on time, so this paper does not include the fabrication and analysis of the digital design.

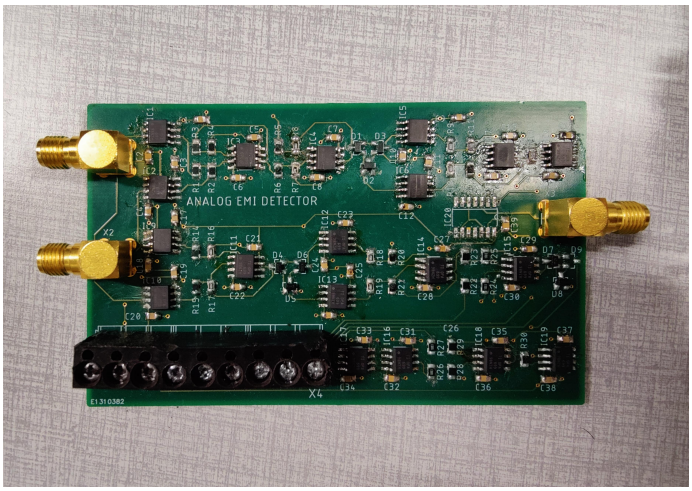

Fig. 7. Fabricated PCB design of the Analogue EMI Detector

IV. Results

Fig. 8 shows an overview of the measurement setup. The Spartan-6 LX45 FPGA is used for transmitting and receiving data at 10MHz. The FPGA also receives the warnings generated by the EMI detector. The system perspective definitions for the EMI detector given in [10] are used for analyzing the performance of the EMI detector. The FPGA calculates the following

- Bit Errors (BERs): These occur when the received bit is not the same as the transmitted one.
- Data True Positives (DTPs) and Channel True Positives (CTPs): DTPs refer to cases where EMD is not strong enough to disturb the transmitted signal, and the EMI detector is not generating warnings. CTPs refer to cases where EMI can disturb the transmitted data, but fortunately, the received data is correct, and no warnings are generated.
- Data False Positives (DFPs) and Channel False Positives (CFPs): DFPs refer to cases where EMI is detected even though data is correct, and EMI is not strong enough to disturb the transmitted data. CFPs refer to detection by the EMI detector when EMI is strong enough to disturb the data, but fortunately, the received data is correct.
- Channel True Negatives (CTNs): They appear when the EMI detector correctly detects EMI in the transmitted signal.
- Channel False Negatives (CFNs): These are the cases when the received data is incorrect, but the EMI detector does not generate a warning.

A shielded room is used to evaluate the performance of the analogue EMI detector, as shown in Fig. 9. The EMD is generated using a log-periodic antenna with a specified frequency range from 30MHz to 1GHz. To make the data transmission lines more vulnerable to EMI, a PCB with a cut in the ground plane is used, as shown in Fig. 10. The receiver side of the data transmission lines is connected to the

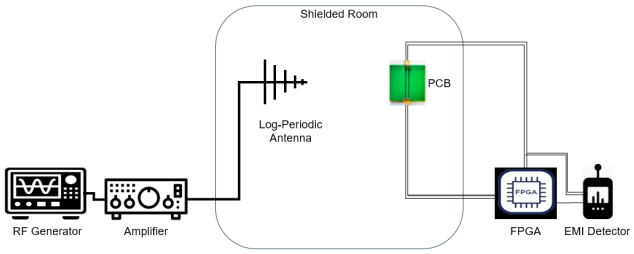

Fig. 8. An Overview of the Measurement Setup

analogue EMI detector and the FPGA, both placed outside of the reverberation room.

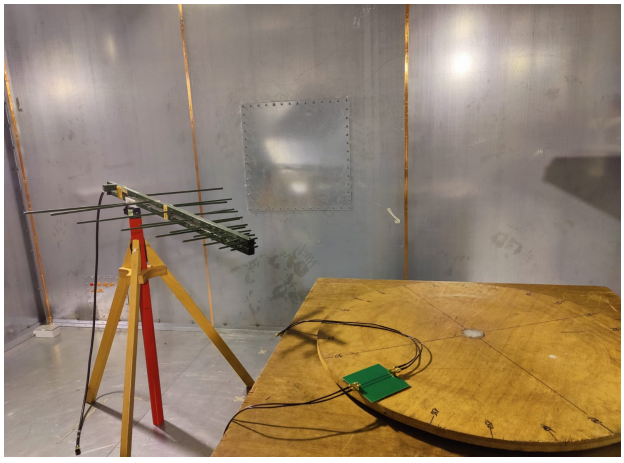

Fig. 9. Analysis Setup for evaluation of the EMI Detector

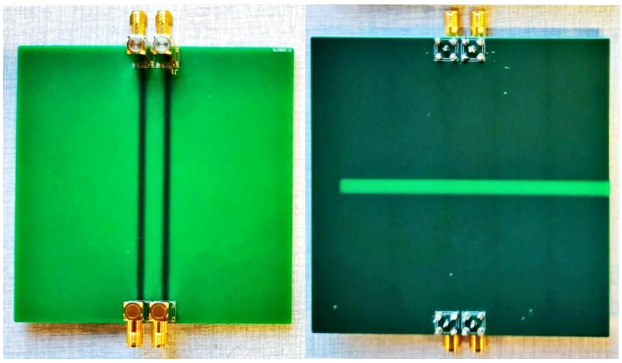

Fig. 10. The PCB Design of data transmission lines

The generator RF power is increased from -10dBm to 5dBm with a step size of 0.1dBm. An amplifier of 35dB is used to amplify the signal. The bit errors in the data transmission lines depend upon both the voltage used for the data transmission and the voltage induced by EMD. Therefore, The EMI detector's response is analyzed by using a Signal to Interference ratio (SIR). The SIR is defined by equation (1).

$$\mathrm{SIR} = 20 \cdot \log_{10}\left(\frac{V_{\mathrm{Sig}}^{\mathrm{RMS}}}{V_{\mathrm{EMI}}^{\mathrm{RMS}}}\right). \quad (1)$$

The response of the analogue EMI detector for EMD at a frequency of 305MHz is shown in Fig. 11. It can be observed that the EMI detector starts generating warnings at the SIR level of 22dB, and it generates warnings for all transmitted bits for SIR below 20.5dB. CTN's are present generated by the EMI detector at SIRs below 15.36dB

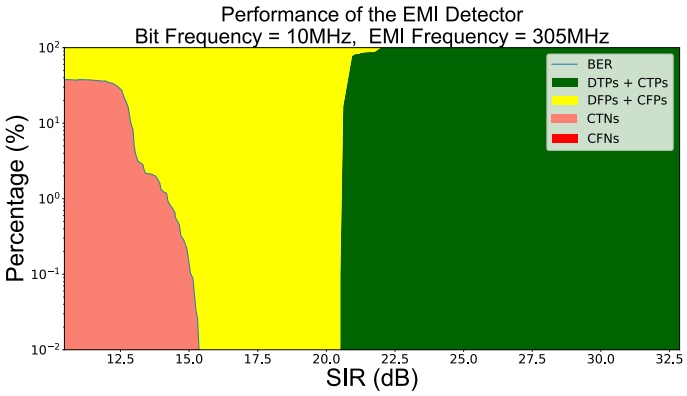

Fig. 11. Response of the Analogue EMI detector at bit frequency=10MHz and EMI frequency=305MHz

In Fig.12, the RF signal is applied with a frequency of 326MHz. It can be observed that the EMI detector is generating warnings below 22.49dB. DFPs and CFPs increase to a hundred percent at 19.45dB, and CTNs start occurring from 14.835dB.

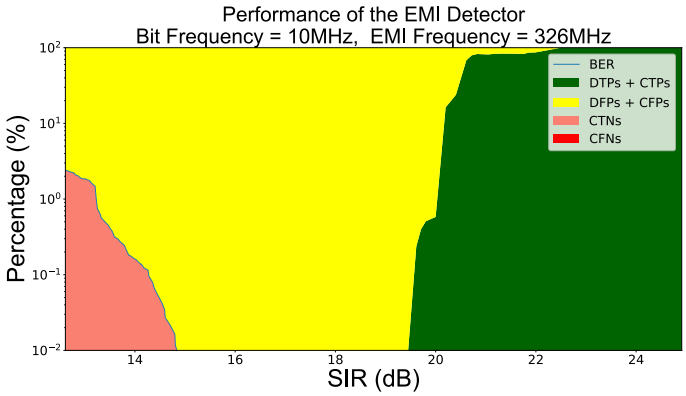

Fig. 12. Response of the Analogue EMI detector at bit frequency=10MHz and EMI frequency=326MHz

The results show that the EMI detector does not generate a warning when SIR is high, and the FGPA receives the data correctly, i.e. DTPs and CTPs. As the SIR decreases, the EMI detector starts generating a warning even when the received data is correct, i.e. DFPs and CFPs. In cases where the SIR power is very high the EMI detector correctly detects BERs, i.e. CTNs. In the performed experiments, there were no cases where the EMI detector was not able to detect BERs, i.e. CFNs. This may be due to the fact that tested frequencies were not a multiple of sampling rate where the theoretical design of the EMI detector was not able to detect. This was not performed due to lower coupling at these frequencies. Results

also show that the EMI Detector starts generating warnings for higher SIR than previous simulations. This is due to the different threshold voltage and voltage levels used for the data transmission in the measurements.

V. Conclusion

The hardware design of the EMI detector is proposed in a digital and analogue form. This paper provides an overview of their designs and analyzes the performance of the analogue EMI detector. The analogue design is tested in a harsh EM environment by varying RF power and frequency. The results show that the EMI detector correctly identifies cases where EMD is interfering with the transmitted data in a wired communication channel. However, warnings are also generated for cases where EMD induced voltage does not cause bit errors, compromising the availability. Future work should focus on testing the analogue EMI detector at multiple frequencies in real EM environments. In addition, future research should focus on a design to reduce DFP of the analogue EMI detector. An analysis is also needed for the digital design of the EMI detector.

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