# Validation of IC Conducted Emission and Immunity Models Including Aging and Thermal Stress

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***Abstract*—Environmental factors such as aging and thermal stress can seriously impact the electromagnetic compatibility (EMC) behavior of an integrated circuit (IC). Standardized conducted emission (ICEM-CE) and immunity (ICIM-CI) models can be used in industry to predict EM behavior at the IC and the printed circuit board (PCB) level. However, these do not take into account the effect of aging and extreme temperature variations. In this paper, a custom IC designed in silicon-on-insulator (SOI) technology, containing several independent analog blocks, is used to characterize the influence of aging and temperature on conducted emission and immunity through measurements and transistor level simulations. Highly accelerated temperature and humidity stress test (HAST) was performed to evaluate aging and its influence on IC parameters. The results show that the passive distribution network (PDN) is only influenced by thermal stress and not HAST aging. The latter mainly affects the active elements in the IC and reduces the conducted emission and immunity levels through intrinsic permanent degradation mechanisms. Furthermore, thermal stress mainly causes drifts in the transistor characteristics (such as threshold voltage and effective mobility) which affect the conducted emission and immunity levels and resulting in soft failures. All drifts/tolerances collected from measurements and simulations are characterized in a way that makes it possible to include them in potential future versions of the ICEM-CE and ICIM-CI standards.**

***Index Terms*—IC, ICEM-CE, ICIM-CI, HAST aging, thermal stress.**

## I. Introduction

INTEGRATED circuits (ICs) are essential components in nearly every modern electronic system. A vital factor in the design process of ICs is estimating if their functionality and electromagnetic compatibility (EMC) characteristics can be guaranteed over their entire lifetime [1]. In that context, both EM emission and immunity of ICs are critical for reducing interference risks at the system level, where several mitigation techniques to suppress emission [2]–[4] and improve immunity [5], [6] of printed circuit boards (PCBs) are reported in literature. Further, it is necessary to analyze and predict the EMC of ICs in harsh environments (e.g. extreme temperatures, humidity, and electrical overstress) before the manufacturing stage [7].

The International Electrotechnical Commission (IEC) has proposed several models to assess the EMC performances of ICs, such as the IC emission model for conducted emission (ICEM-CE) and the IC immunity model for conducted immunity (ICIM-CI), which are published in IEC62433-2 [8] and IEC62433-4 [9], respectively. Those models can be generated either through a black box or a white box approach. The former does not require the knowledge of the internal structure of the IC, while the latter approach provides the models in a simulatable form [10]. As shown in Fig. 1a, the ICEM-CE model consists of a passive block called the passive distribution network (PDN) and an active block known as the internal activity (IA). The former describes the power supply network of an IC and shows the significant coupling paths from the noise source to the external pins of the IC [11], whereas the IA describes the activity of the internal block of the IC as a current source.

As observed in Fig. 1b, the PDN of the ICIM-CI model is identical to that of the ICEM-CE and can be modeled using lumped passive elements. Additionally, the immunity model also comprises the immunity behavior (IB) block which is usually characterized as a look-up table that can be coupled to a comparator to output a pass/fail criterion based on the injected power [12]. The main limitations of these models are that they do not include the relevance of aging and thermal stress that can cause a drift in the EM conducted emission and susceptibility levels.

Due to natural aging, ICs can be affected by intrinsic failure mechanisms, such as gate oxide defect, electromigration, hot carrier injection (HCI) and negative bias temperature instability (NBTI) [13], [14]. The latter two are the most prevalent permanent degradation effects and can be analyzed by accelerated life tests [15]. Furthermore, temperature variations can temporarily influence MOSFET parameters such as threshold voltage ($V_{th}$) levels, effective mobility ($\mu_{eff}$), transconductance, and saturation currents [16]. These can trigger soft failures and can have significant impact on the stability parameters (leakage current, noise margin, jitter, operating frequency etc.) of the IC [17].

In literature, researchers have developed conducted emission models using de-embedding measurement techniques [18] and

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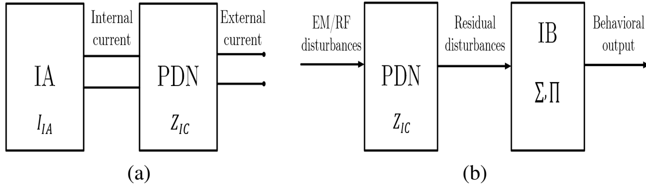


Fig. 1. Modeling framework of: (a) ICEM-CE; (b) ICIM-CI.

simulation tools [19] for microcontrollers and phase locked loops (PLLs). Few researchers have also introduced an alternative approach to model the IA block for oscillators [20]. In addition, some works have been carried out to develop ICEM models up to 3 GHz and the impact of high temperature on the emission levels has been analyzed [21], [22]. The effect of aging on the conducted emission of switches were studied in [23] and reliability models for field programmable gate arrays (FPGAs) were developed in [24] and [25] to predict failures over their entire life cycle.

As far as immunity is concerned, some researchers developed multi-port models to extract the conducted immunity profiles of analog circuits [26], [27]. The ICIM-CI model has also been extended to include the effect of transient EM disturbances [28]. Moreover, conducted immunity models were proposed to predict the long-term immunity of PLLs using accelerated life tests [29]. A recent study proposed an EM-thermal model to characterize the conducted immunity of an input/output (I/O) element for FPGAs [30].

To the best of the authors' knowledge, the influence of both aging and thermal stress on EMC models applicable on silicon-on-insulator (SOI) ICs has not been investigated so far. Therefore, in the current study, the ICIM-CI and ICEM-CE models were developed for independent analog circuits that were integrated into a custom-designed IC. Through measurements and transistor level simulations, the effect of extreme temperature deviations and accelerated aging were included into either the passive or active blocks of the proposed models.

The remainder of the paper is organized as follows. Section II describes the custom-designed IC and the PCB variants as well as the independent analog blocks used for conducted immunity and emission testing. This section also outlines the measurement setups for accelerated life tests and immunity/emission measurements under thermal stress. Sections III and IV present the experimental and simulation/modeling results for conducted emission and immunity, respectively. Finally, the conclusions of this study are presented in Section V.

## II. Materials and Methods

This section introduces the IC and PCB variants designed for the purpose of this study. Then, the circuits designed for conducted emission and immunity are described. It is followed by the highly accelerated life testing performed to represent the aging of the custom IC. Furthermore, the experimental test setup to characterize the IC conducted emission and immunity is also described.

### A. Custom IC and PCB Variants Design Description

For the purpose of this study a 1.52 mm × 1.52 mm chip (PETER_ESEO) [31], including various analog structures, was fabricated in SOI CMOS 180 nm 5 V technology. The design and layout of all the integrated blocks were performed using Cadence Virtuoso. The core is surrounded by a core-limited padring that is powered by the global power supply ($V_{DDO}$). It consists of 52 pads with identical N-MOS based ESD protection devices connected to both $V_{DDO}$ and the global ground ($G_{NDO}$). All structures have an isolated power supply pad ($V_{DDI}$) and a separate ground ($G_{NDI}$), due to the use of SOI technology. The output of each circuit is connected to an analog pad and an ESD protection circuit which will clamp the generated signals that are not within the 0 to 5.5 V range. The internal ESD circuits of the $V_{DDI}$/$G_{NDI}$ and analog I/O pads include N-MOS transistors with gate-to-source resistors to reduce the overall gate leakage current.

The die samples were packaged in a 64-pin ceramic quad flat package (CQFP). All power supply and ground pads were bonded to the package pins with spacing in between them to minimize the effect of mutual inductive coupling. This makes it possible to not only inject more power into the supply pads but also to monitor high frequency signals [32].

To test the conducted emission and immunity of the IC, a 13 cm × 13 cm 4-layer FR4 PCB, was designed according to IEC 61967-4 [33] and IEC 62132-4 [34] using Altium Designer. The PCBs were not overloaded with non-linear components, to restrict uncontrolled RF/EM behavior [35]. All isolated grounds of the IC were connected to the global ground. Specifically, for the circuits tested for immunity, a 470 Ω resistor was added in series to its output pin in order to limit high voltage signals from being re-injected into the IC or the oscilloscope. Only for the conducted emission circuit, the $G_{NDI}$ pin was connected to 49 Ω and 1 Ω resistors in compliance with the 1−Ω method of IEC 61967-4 [33].

In addition, a second 13 cm × 13 cm 4-layer FR4 PCB variant was designed to measure the (scattering) $S$-paramerters of the IC pins. The IC was mounted at the center of the PCB with its pins connected to several micro-miniature coaxial (MMCX) through-hole female connectors with a characteristic impedance of 50 Ω covering a frequency range from DC to 4 GHz. Instead of the standard SMA connectors, MMCX were used due to their compact size, which makes it practicable to test all IC pins on the same PCB. The injection traces were placed radially in a circle, with a 47 mm individual primary length, to keep the distance between each MMCX and IC pin equal. More details of the designed PCB can be found in [32].

For accurate $S$-parameter measurements, it is essential to design a calibration board. This makes it possible to extract the impedance profile of the IC pin without the effect of the PCB traces. A 10 cm × 10 cm 4-layer FR4 calibration PCB was designed and panelized with the same PCB substrate as the $S$-parameter board. The calibration technique adopted was the short-open-load-thru (SOLT), generally providing an accuracy of up to 4 GHz [36]. The primary length of the short, open, and load traces was set to 47 mm, while the thru trace was fixed to 94 mm. As far as the load is concerned, a high precision

50 Ω (0402) resistor was used for termination.

## B. Conducted Emission Circuit Design

To investigate conducted EM emission at IC level, a $H$-clock tree noise circuit was included in the PETER_ESEO die. It consists of 85 analog non-inverting buffers with identical aspect ratios. It has a total of 4 stages and 64 output branches, which were left floating. The schematic is displayed in Fig. 2a. One branch of the $H$-clock tree was connected to the input analog pad and the clock signal ($V_{clk}$) was injected externally through it. The routing of the circuit was kept highly symmetrical in order to maintain equal propagation delays in each branch of each level. Non-inverting buffers were used instead of simple inverters to provide better sensitivity and ensuring all routed signals remain in-phase, as well as to further avoid noise cancellation [37].

When a clock signal is provided to the input of the $H$-clock tree, it generates high frequency conducted EM disturbances, specifically in its power supply and ground rails. An on-chip sample and hold (*S&H*) voltage sensor based on deep-downsampling was also included in the IC to characterize these coupled EM disturbances by transposing them to much lower frequencies [38]. The voltage sensor is made up of the following blocks (Fig. 2b from input to output):

- a resistive divider including compensation capacitors and an attenuation ratio fixed to 1/2;
- a sampling cell containing a storage capacitor and a CMOS pass gate driven by an external clock, with a 1 GHz bandwidth;
- a unity gain differential Miller amplifier including a current source and a start-up circuit with a 100 MHz bandwidth.

The voltage sensor principle is based on intentional aliasing, operating much below the Nyquist criteria, in order to transpose high frequency signals down to a few MHz. The influence of parasitic elements such as the pad capacitance, package and bonding can be excluded at such low frequencies [39]. Hence, the output signal amplitude is a linear function of the input signal amplitude. The Miller amplifier aspect ratios were optimized according to Jespers and Murmann sizing methodology provided in [40] using pre-determined SPICE generated look-up tables and explicit MATLAB functions [41].

As illustrated in Fig. 2c, the supply rail $V_{DDI1}$ of the $H$-clock tree noise circuit is connected to the analog input of the *S&H* voltage sensor. When a square signal with a constant frequency is injected into the $A_{in}$ of the $H$-clock tree, the switching activity of the buffers produces conducted noise which propagates to the $V_{DDI1}$ or $G_{NDI1}$. Conducted emission measurements were carried out using the 1 Ω probe [33] placed at the $G_{NDI1}$ pin of the $H$-clock tree. Furthermore, the *S&H* output peak voltage is directly proportional to the conducted emission generated in the $V_{DDI1}$. The $V_{DDI2}$ and $G_{NDI2}$ of the voltage sensor were entirely isolated from the conducted noise and was verified to have no impact on the emission analysis.

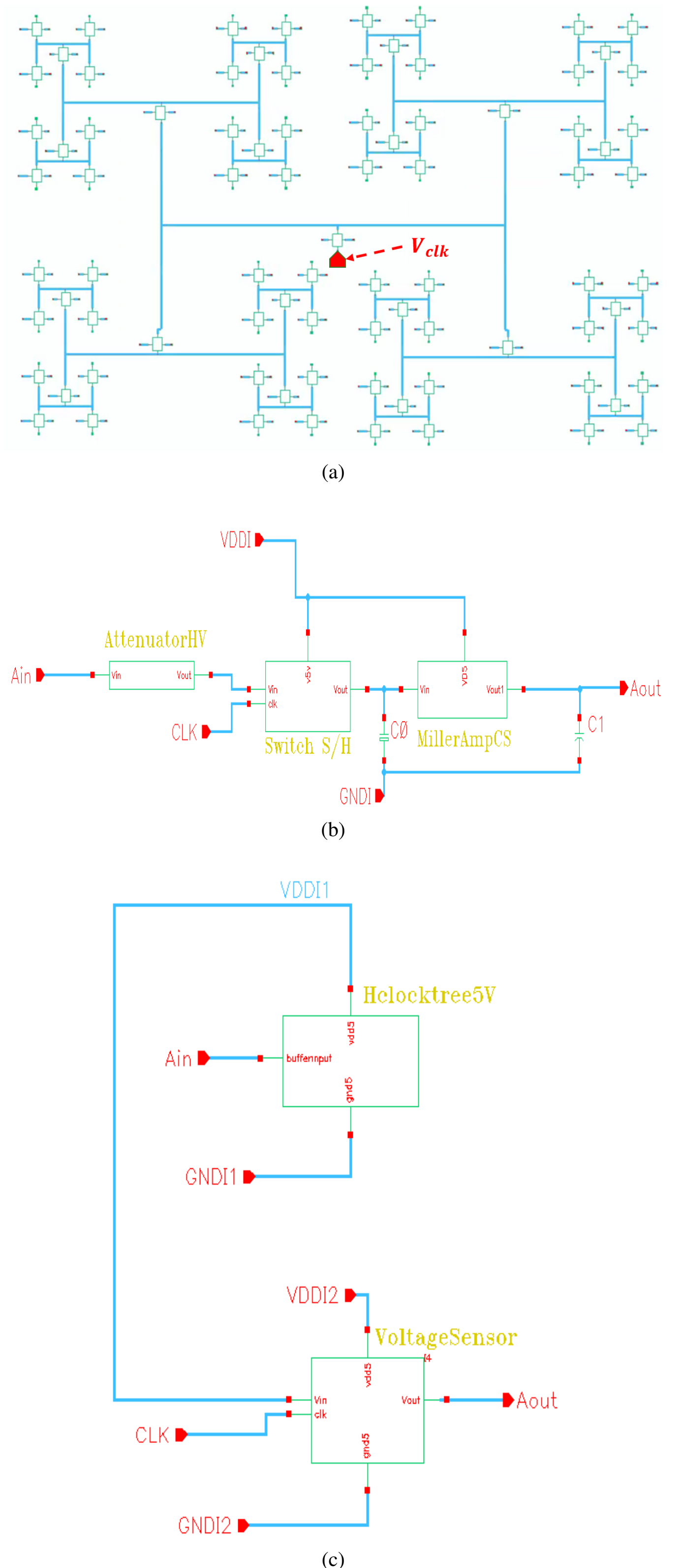


Fig. 2. Conducted emission schematics: (a) $H$-clock tree; (b) *S&H* voltage sensor; (c) combined emission circuit.

## C. Conducted Immunity Circuit Design

To analyze the conducted EM immunity, two independent analog blocks integrated into the IC were selected. Those are a 3-stage current starved voltage controlled oscillator (CSVCO)

and an analog set/reset (*S*-*R*) latch. The former is an integral part of mixed-signal ICs such as phase-locked loops (PLL), and the latter is utilized in sequential memory circuits. The power supply of the mentioned structures are prone to conducted EMI, which affects their performance characteristics [42]. Both circuits have separated V$_{DDI}$ and G$_{NDI}$ rails to avoid any interference or coupling during immunity testing.

As displayed in Fig. 3a, the CSVCO topology includes externally biased MOSFETs that control the current provided to its inverter stage. The biasing supply (V$_C$) is connected to those MOSFETs to minimize power consumption and tune the frequency range [43]. For this study, the V$_C$ is biased to 1.8 V and the 3-stage CSVCO generates a stable sinusoidal signal operating at 703 MHz.

A 3-stage digital frequency divider (FD) circuit is added at the output stage of the oscillator to lower the fundamental frequency of the generated signal. The FD is powered by V$_{DDO}$, which is isolated from the oscillator individual power supply and allows monitoring the frequency at the analog output pad without filtering effects caused by the parasitic pad capacitance. The maximum operating clock frequency of the FD was equal to 900 MHz.

Latches are single bit storage elements used in computing and data storage. The *S*-*R* latch is an asynchronous bistable multivibrator which works independently of the control signals and relies only on the $S$ and $R$ inputs [44]. The latch comprises two NOR gates with a cross-feedback loop from the outputs Q and QB (Fig. 3b). All the used MOSFETs have identical aspect ratios. An analog version of the *S*-*R* latch was designed to be able to utilize an isolated power supply and ground. To test the conducted immunity of the latch, EMI was injected into the power supply whereas both outputs were monitored to check if the latch enters into a metastable state.

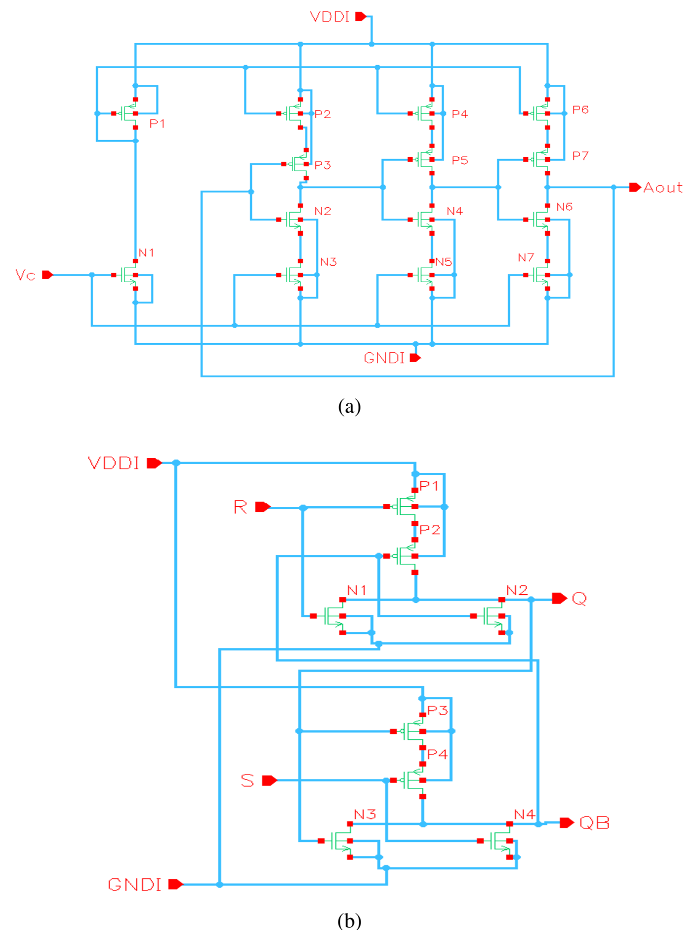


Fig. 3. Conducted immunity test circuits: (a) 3-stage CSVCO; (b) analog *S*-*R* latch.

### *D. Aging of ICs*

To investigate the impact of aging on the emission and immunity behavior of ICs, accelerated life tests are usually performed in industry. High-level stress conditions such as extreme high temperature or voltage, are applied for a short period of time to accelerate the damage rate for relevant wear-out failure mechanisms such as NBTI and HCI [45]. The most frequently used accelerated tests to induce such degradation mechanisms are high and low temperature operating life tests (HTOL and LTOL) [46], and temperature humidity bias test (THB) [47]. The latter is a method of electronic reliability testing using temperature and relative humidity (RH) as the environmental parameters. The test is carried out at 85 °C and 85% RH continuously for 1000 hours to predict the operational lifetime of the device up to 25 years.

Highly accelerated temperature and humidity stress test (HAST) is a more accelerated version of the THB test (causing equivalent failure modes) and is performed at 130 °C and 85% RH continuously for only 96 hours [48]. The purpose of HAST is to evaluate the humidity resilience of a component or an encapsulated IC by increasing the water vapor pressure to an extremely high level above the partial water vapour pressure inside the IC. Hence, this test causes a rise in component contact resistance due to moisture corrosion and insulation deterioration.

HAST was selected herein as the accelerated life test to evaluate the effect of aging on the conducted emission and immunity of the PETER_ESEO IC. As illustrated in Fig. 4, the immunity/emission and $S$-parameter PCB variants along with several packaged ICs were placed in a HAST chamber (ESPEC EHS-412M) at a constant 130 °C temperature and 85% RH for 96 hours. For the entire duration of the test, the global power supply and the isolated supplies of the $H$-clock tree, *S&H* voltage sensor, *S*-*R* latch and the CSVCO circuits in the IC were biased to 5 V using external DC power supplies through high temperature cables. At the end of the test, all PCBs and ICs were still operational with no visible damages. The only noticed observable effect was that the PCB traces connected to the biased IC pins had different colors changing from green to black due to corrosion.

### *E. Conducted Immunity and Emission Measurement Test Setup*

The direct power injection (DPI) method is commonly used to characterize the conducted immunity of the IC from 150 kHz to 1 GHz frequency spectrum [34]. The immunity behavior of ICs is established based on the minimum transmitted power level that is required at a specific frequency

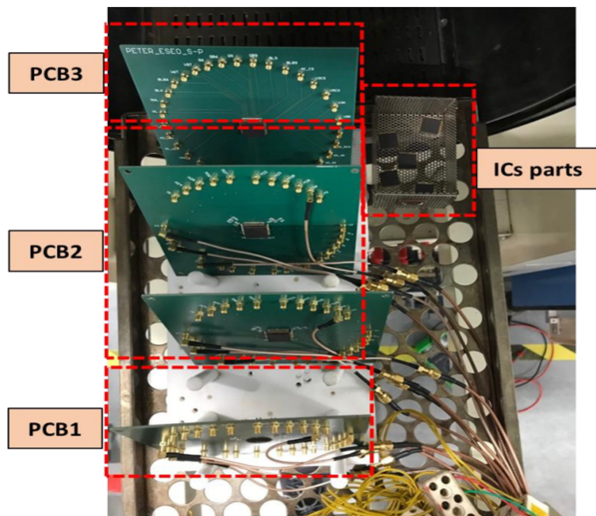


Fig. 4. Aging of ICs in HAST chamber.

within a given RF range to cause IC failure [49]. The DPI measurement setup is depicted in Fig. 5. The test bench includes a RF generator (Agilent N5183A), a series power meter (Agilent E4419B), a bi-directional coupler, a RF power amplifier (Prana AP32DT120), a multi-channel DC power supply (N6700B), a bias-tee (ZFBT-6GW+), an oscilloscope (Keysight DSOS204A), an arbitrary waveform generator (Agilent 33250A), a signal analyzer with a LabView interface (Agilent N9010A), extreme temperature cables (Amphenol-RF 095-902-466-004), and a SATIMO thermal oven.

The analog *S-R* latch and the CSVCO were tested using this setup in order to analyze their conducted immunity behavior. The RF generator produces the continuous wave EM disturbance that flows through the bi-directional coupler and is superimposed over the 5 V provided by one of the DC power supply channels via a bias-tee into the $V_{DDI}$ pin of the tested circuit. The remaining channels of the DC supply were connected to the global $V_{DDO}$ and the $V_C$ of the CSVCO at 5 V and 1.8 V, respectively. The power meter provided the injected power from the measured forward and reflected power magnitudes. The amplifier was used to stabilize the injected signals at higher power levels (above 20 dBm). The device under test (DUT) was placed inside the oven and the output pin of the tested circuit was connected to the oscilloscope (1 MΩ) via high temperature cables. The LabView interface was used to control the entire test setup and apply a failure criterion on the output signal using mask testing. The latter involved fixing a mask up to a tolerance limit on the output signal in both directions (lower and higher). Then, the statistical failure rate i.e., the output signal leaving the area of the oscilloscope mask, was averaged over a specific time slot.

An AC decoupling capacitor was not used and routed on the tested DPI PCB variants. This was specifically done to avoid any additional effects caused by external components when subjected to thermal stress, seeing that no external components were required to ensure proper operation of the integrated blocks. In the DPI method, RF power was injected into the IC power supply pins using external bias-tees.

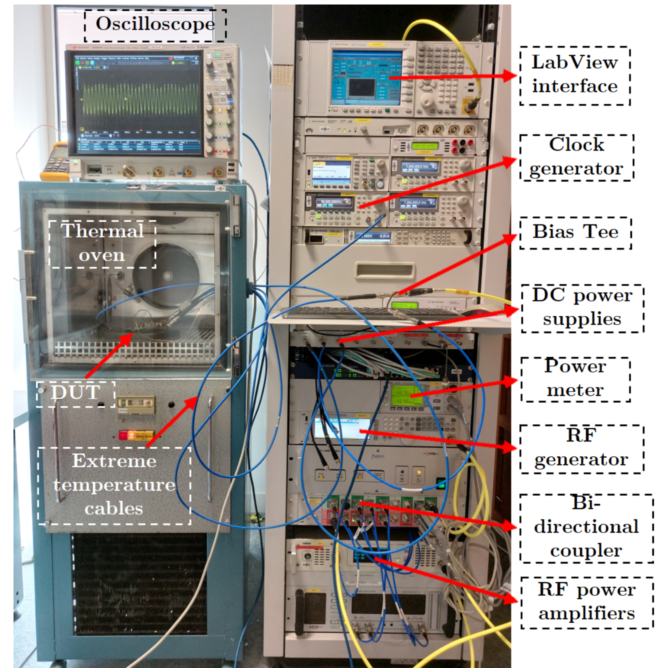


Fig. 5. DPI experimental test setup.

The above-mentioned measurement setup was also utilized for conducted emission testing. The $V_{DDI}$ rails of the $H$-clock tree and voltage sensor were biased to 5 V. One of the channels of the arbitrary wave generator was utilized to inject a square wave into the analog input pin of the $H$-clock tree and the second channel generated the clock signal for the *S&H* voltage sensor. The current activity of the $G_{NDI}$ of the noise circuit and the output peak voltage of the *S&H* sensor were monitored through the oscilloscope channels at 50 Ω and 1 MΩ, respectively.

## III. Conducted Emission Results and Discussion

This section deals with the conducted emission analysis of the $H$-clock tree and the extraction of the ICEM-CE model, comprising the PDN and IA blocks. Further, the effect of aging and thermal stress are analyzed in measurements and included in the emission model. The $H$-clock tree was subjected to a square wave input of 50 MHz frequency, 50% duty cycle, 10 ns rise/fall times and 5 V amplitude. The clock of the *S&H* voltage sensor was set to 999 kHz frequency, 3% pulse width, and 5 V amplitude. The voltage sensor with these clock characteristics transformed the 50 MHz switching activity emitting from the $H$-clock tree into to a 50 kHz output voltage signal. To characterize the effect of aging, all measurements of the fresh and aged DUTs were carried out at ambient temperature (25 °C). Conversely, to analyze the effect of thermal stress on the conducted emission of the noise circuit, measurements were performed on fresh DUTs at ambient and extreme temperatures (i.e., −40 °C and 120 °C). The respective minimum and maximum temperatures were chosen since they conform to the temperature limits of all the components soldered on the tested PCBs.

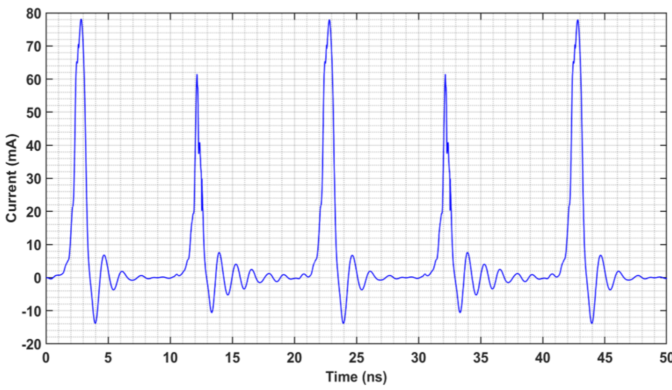


Fig. 6. Simulated internal transient current (IA) generated by the $H$-clock tree and monitored at the $V_{DDI}$.

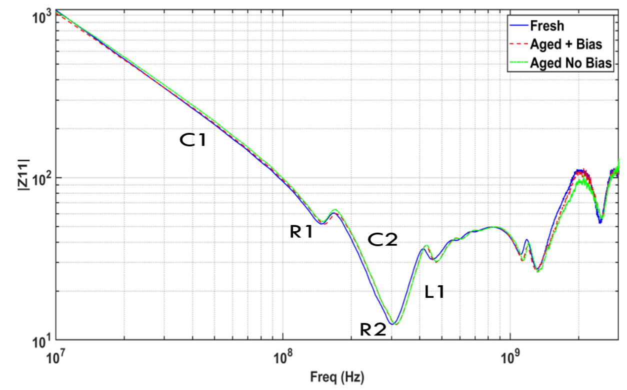


Fig. 7. Measured impedance profile of $V_{DDI}$ of $H$-clock tree with aging.

### A. Extraction of the ICEM-CE Model

For the ICEM-CE modeling of a commercial IC, where the latter is considered a black box, an image of the internal current is extracted using measurement tools and impedance profiles from the external current. However, since the IC under test is custom-designed, the internal current was extracted using Cadence Virtuoso (simulation-based transistor-level approach). A hierarchical parasitic extraction was performed for the IC to better approximate the realistic behavior of the dynamic current. The switching of the analog buffers in the $H$-clock tree generates a conducted noise emitted through its $V_{DDI}$ or $G_{NDI}$ rail. Due to a stable input frequency of 50 MHz, the IA dynamic current emission waveform consists of periodic spikes having the same fundamental frequency. The internal current profile of the $H$-clock tree is shown in Fig. 6. The IA time domain characteristics exhibit a 1 ns rise time ($t_r$), a 20 ns period, a 2.5 ns pulse width and an overall peak-to-peak current of 94.5 mA. Each period has two consecutive current spikes with an amplitude of 78.4 mA and 61.3 mA. The extracted internal current was then fed as a netlist to the independent current source to model the IA block of the ICEM-CE model.

The electrical behavior of the PDN is given by its complex impedance and can be modeled using lumped passive R, L, and C elements. To determine which passive elements are required to model the PDN upto a certain frequency, the $t_r$ of the internal current is a critical parameter. The bandwidth capable of dealing with this $t_r$ can be determined using [18]:

$$F_{max} = \frac{0.35}{t_r} \tag{1}$$

Harmonics above $F_{max}$ are considered low enough not to generate considerable emission levels. Hence, the frequency limitation of the PDN is equal to 350 MHz.

A vector network analyzer (VNA) was used to measure the one-port $S$-parameters ($S_{11}$) of the $V_{DDI}$ pin of the $H$-clock tree. Furthermore, a calibration board, adopting the SOLT method, was utilized to accurately measure the correct $S_{11}$ profile between 10 MHz to 3 GHz. The impedance parameters ($Z_{11}$) results were then extracted from the $S_{11}$. The impedance profile of the $H$-clock tree power supply network is shown in Fig. 7. The frequency response of the impedance up to 350 MHz is divided into several parts. Below 120 MHz, the impedance is capacitive (C1). The impedance becomes resistive at 150 MHz (R1) and 315 MHz (R2). The latter has a lower value and is the actual impedance at the resonant frequency, where the phase crosses zero. Between 150 to 300 MHz a steeper capacitive (C2) impedance effect is observed. The reason for the parasitic resonance is due to the $V_{DDI}$ rail of the $H$-clock tree connected inside the IC to the input of the voltage sensor. The first stage of the sensor includes an attenuator with compensation capacitors, which causes the parasitic resonances noticed in the impedance profile. From 320 MHz until 400 MHz the impedance becomes inductive (L1) and can be computed at a given frequency with in this range.

The ICEM-CE simulation setup is depicted in Fig. 8. It includes an independent current source, which represents the IA block of the ICEM model. The block capacitance (C1) was measured through the VNA when the $V_{DDI}$ rail of the $H$-clock tree was biased with 5 V. The difference in the capacitance from the unbiased version was found to be 10 pF. The first order R, L, and C parameters (R2, C2, R3, C3, L1, L2) were extracted from the $Z_{11}$ profile and they make up the PDN of the ICEM model. Further, to have a better correlation between the conducted emission measurements and model, the die to ground capacitance (C4) of 1.2 pF was included in the latter. The ICEM-CE simulation setup also includes a 5 V DC source and a 1 Ω resistor (R4) in series with its 1 nH parasitic inductance (L4) connected to the ground. Since the PCB trace has a length of 47 mm, it can generate a 47 nH (1 nH/mm) parasitic inductance (L3), which was added in series to the 49 Ω resistor (R5). Finally, the oscilloscope was modelled by a 50 Ω resistor (R6) and its 15 pF parasitic capacitance (C5) which affects the peak of the output signal in measurements.

The external current activity extracted from the ICEM-CE simulation setup and through measurement using the 1−Ω method are illustrated in Fig. 9. A significant correlation between the extracted and measured current was noticed. The maximum peak-to-peak current of the former was 2.6% higher than the latter. However, the measured current included some minor parasitic inductance effects noticed at the consecutive spikes which could be due to measurement uncertainty. Inter-

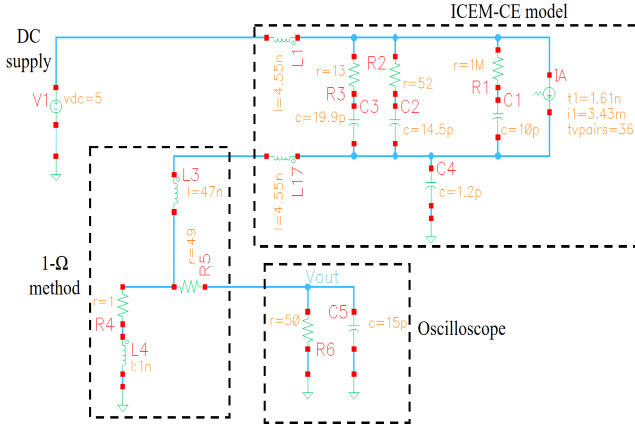


Fig. 8. ICEM-CE simulation setup.

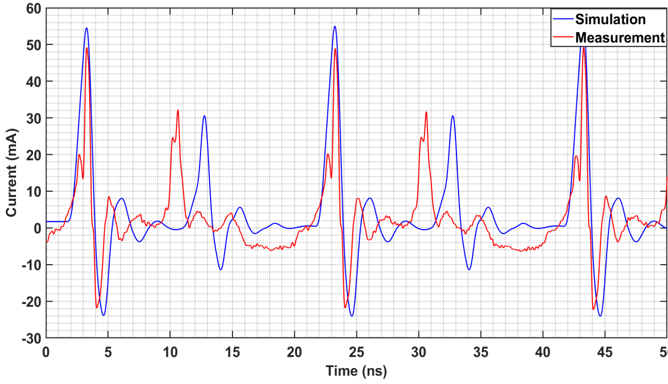


Fig. 9. Comparison of the external current extracted through the ICEM simulation setup and 1-Ω measurement.

estingly, the peak-to-peak internal current (Fig. 6) was only 20.3% (16 mA) higher than the measured external peak-to-peak current (Fig. 9). In comparative literature, the ICEM-CE model's internal current (IA) is considerably higher (120% or above [10], [18]–[20], [24]) than the measured external current extracted through the 1-Ω method. The filtering effect of the PDN is responsible for such lower peak values of the external current. Hence for our custom-designed IC, the PDN has a lower filtering effect (20.3%) on the internal switching current.

## B. Influence of Aging on Conducted Emission

As mentioned in Section II-D, HAST testing was performed on the DUT (biased and unbiased) to evaluate the effect of aging on the conducted emissions generated by the $H$-clock tree. All $S$-parameter and conducted emission measurements were carried out at ambient temperature on fresh and aged ICs to find out if the PDN or/and the IA blocks of the ICEM model are impacted by aging. Results shown in Fig. 7, demonstrate that HAST aging in both biased and unbiased ICs causes negligible variation in the $Z_{11}$ profile over the entire frequency range. There exists a minor variation in the $Z_{11}$ for frequencies above 1 GHz but this can be discarded due to measurement uncertainty. These results demonstrate that aging due to HAST

TABLE I
VARIATION IN CONDUCTED EMISSIONS WITH AGING (HAST); THE *italic* VALUES ARE EXTRACTED BY EXTRAPOLATION FROM MEASUREMENTS

| Sample | External peak-to-peak current | Internal peak-to-peak current | *S&H* sensor peak-to-peak voltage |
|---|---|---|---|
| Fresh | 78.54 mA | 94.50 mA | 1.46 V |
| Aged 1 | 70.95 mA | *85.35* mA | 1.39 V |
| Aged 2 | 71.81 mA | *86.39* mA | 1.40 V |
| Aged 3 | 72.32 mA | *87.01* mA | 1.42 V |
| Aged 4 | 72.03 mA | *86.66* mA | 1.41 V |

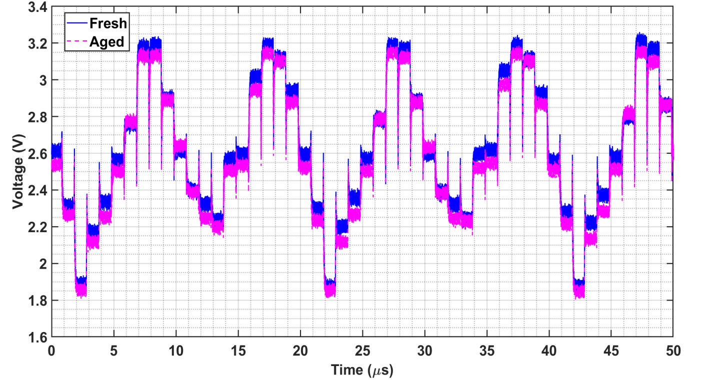


Fig. 10. Effect of aging on the clocked output voltage of the sensor.

has no considerable impact on the PDN of the ICEM-CE model.

Contrarily, the conducted emission measurement results using the 1-Ω method revealed the induced effect by aging due to HAST on the external maximum peak-to-peak current levels. For the duration (96 hours) of the HAST aging test the power supply of some circuits were connected/biased to a 5 V power supply (Aged 1, Aged 2), while some ICs were left unconnected/unbiased (Aged 3, Aged 4). This was done to figure out if voltage biasing while aging has an impact on the conducted emission levels. Several ICs were tested for the sake of repeatability.

The time domain characteristics of the fresh and aged samples were the same but with reduced peak current levels for the aged ones (Table I). The average external peak-to-peak current of all the aged samples (71.52 mA) was 9.8% lower than the fresh version (78.54 mA). Since, aging had no impact on the PDN, the only possible explanation for the reduced external conducted emission levels is due to the decreased amplitude of the internal current. Aging due to HAST triggered degradation mechanism NBTI, impacting the switching activity of the buffers in the $H$-clock tree, and hence, impacting the internal current emission levels. Since HAST aging was performed at elevated temperatures, HCI did not occur since it degrades MOSFETs characteristics at minimum temperatures. As indicated in Table I, the peak-to-peak internal current values of the aged samples were extrapolated from measurements. Voltage biasing had no impact on the reduced current emission levels after aging.

The *S&H* voltage sensor was used in random acquisition mode and intentionally under-sampled the 50 MHz current

switching activity of the $H$-clock tree down to 50 kHz. Although, it was not possible to reconstruct the shape of the input signal in random acquisition mode, the histogram type output voltage signal could indicate RF distortions in the conducted emission signal. The output voltage waveform of the fresh and aged sensors is shown in Fig. 10. No such distortions were observed in the output waveform. More importantly, the average output peak-to-peak voltage of the aged samples (1.40 V) was 60 mV lower than the fresh samples (1.46 V) (Table I).

To validate that aging only affected the internal switching activity of the $H$-clock tree, a separate/identical *S&H* voltage sensor (integrated into the IC) was tested after aging. No considerable variation in amplitude or DC offset was observed in the output signal when subjected to a 50 MHz input sine wave. This verified that the reduction in peak output voltage amplitude was due to the $H$-clock tree. It was checked that the spectral content of the external current did not vary with aging. Since the PDN does not change with aging either, a constant coefficient of proportionality can be established between the external and the internal (IA) peak values whatever the IC state (fresh/aged). This coefficient can be extracted from simulations of the fresh IC and reused for aged ICs which cannot be simulated. Therefore, the IA block could be modified to include that coefficient of aging.

### C. Influence of Thermal Stress on Conducted Emission

In comparison with aging, thermal stress can temporarily raise junction temperatures of CMOS transistors in the tested circuit and create a drift in their $V_{th}$, $\mu_{eff}$, and drain current levels [50]. Although no permanent degradation mechanisms occur, these drifts can cause unexpected conducted emission levels. As described in Section III-A, $S$-parameter measurements were performed on fresh PCBs at ambient and extreme temperatures (−40 °C and 120 °C) to characterize the effect of thermal stress on the $Z_{11}$ profile of the $V_{DDI}$ of the $H$-clock tree. This time, the VNA was calibrated by placing the calibration board at extreme temperatures as well, to exclude thermal influence on the cables, the PCB traces and the MMCX connectors.

The values of passive elements, which define the PDN block of the ICEM model, are measured till 400 MHz to extract the first order circuit. The lumped parameters in Fig. 11 directly correspond to the ICEM-CE schematic in Fig. 8. As seen in Fig. 11, the R, L, and C values of $Z_{11}$ increase with rise in temperature. Interestingly, the effect of thermal stress on the $Z_{11}$ over the entire frequency range was significant (38% span for R2), which could not be discarded. This implies that thermal stress has an impact on the PDN of the ICEM model and all extreme values (shown in Table II) of the passive elements need to be included.

Similar to aging, the conducted emission measurement results using the 1-Ω method revealed a variation of the maximum external peak-to-peak current levels due to thermal stress. As noticed from Table III, a rise in temperature substantially decreased the external peak current levels. With respect to ambient temperature, a deviation of +14% and −26% of the external peak-to-peak current was observed at −40 °C and 120 °C, respectively.

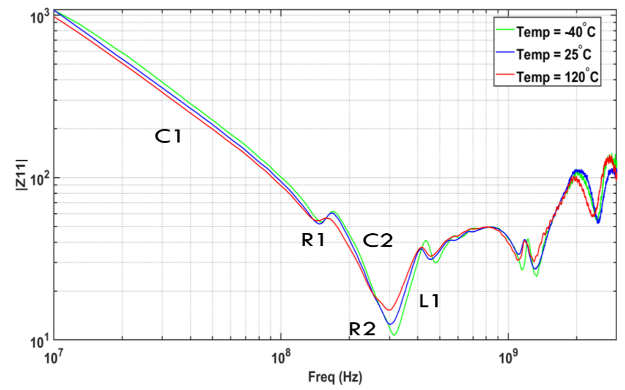


Fig. 11. Influence of temperature on the measured impedance profile of the $V_{DDI}$ of the $H$-clock tree.

TABLE II
DEVIATIONS IN PDN PARAMETERS EXTRACTED AT THE $V_{DDI}$ OF THE $H$-CLOCK TREE DUE TO THERMAL STRESS

| Component | T = -40 °C | T = 25 °C | T = 120 °C |
|---|---|---|---|
| C1 | 13.2 pF | 14.5 pF | 15.9 pF |
| R1 | 51.5 Ω | 52 Ω | 54 Ω |
| C2 | 17.7 pF | 19.9 pF | 21.5 pF |
| R2 | 11 Ω | 13 Ω | 16 Ω |
| L1 | 8.6 nH | 9.1 nH | 9.7 nH |

TABLE III
VARIATION IN CONDUCTED EMISSIONS WITH THERMAL STRESS

| Temperature | External peak-to-peak current | Internal peak-to-peak current | *S&H* sensor peak-to-peak voltage |
|---|---|---|---|
| -40 °C | 89.55 mA | 99.71 mA | 1.49 V |
| 25 °C | 78.54 mA | 94.50 mA | 1.46 V |
| 120 °C | 58.09 mA | 83.44 mA | 1.38 V |

To further verify that thermal stress affects not only the PDN but also the IA block of the ICEM model, transistor level simulations were carried out in Cadence Virtuoso for different temperatures including the thermal behavior of external passive elements. The internal current at the $V_{DDI}$ node of the $H$-clock tree was monitored at nominal and extreme temperatures. As illustrated in Fig. 12, the amplitude of the internal current was found to have an inverse variation with thermal stress. Further, the internal current peak-to-peak found at extreme temperatures through simulations are included in Table III. Although variations in the internal current exist due to temperature, the deviations are lower compared to the externally measured current. Therefore, the dependence of the PDN and the 1 Ω output resistor on temperature enhances the effect of thermal stress on the external peak current levels. Indeed, the same method as the one related to aging can be applied for thermal using another coefficient of proportionality for extreme temperatures.

The output voltage waveform of the *S&H* voltage sensor is shown in Fig. 13. Similar to aging, no distortions were noticed in the output signal. The output peak-to-peak voltage levels

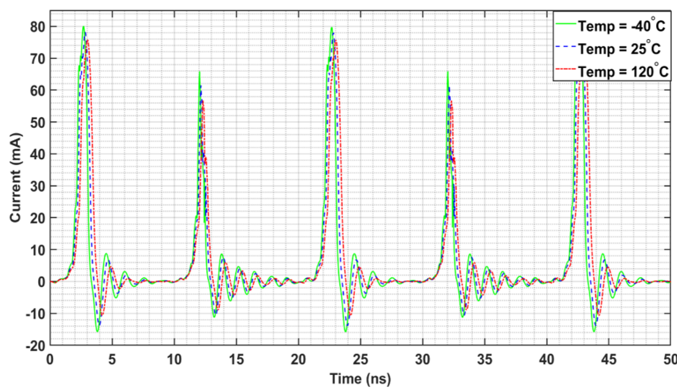


Fig. 12. Influence of temperature on the simulated internal transient current (IA) generated by the $H$-clock tree and monitored at the $V_{DDI}$.

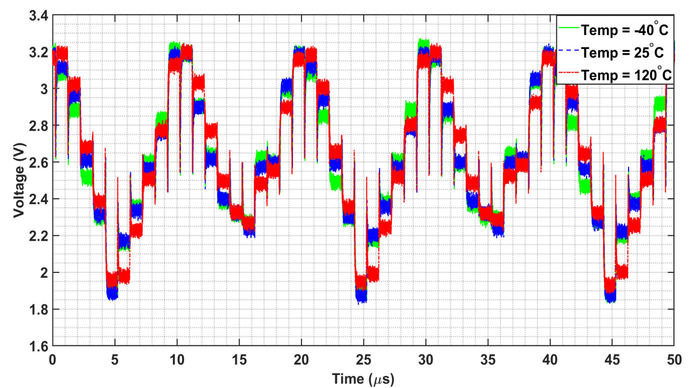


Fig. 13. Influence of thermal stress on the clocked output voltage of the sensor.

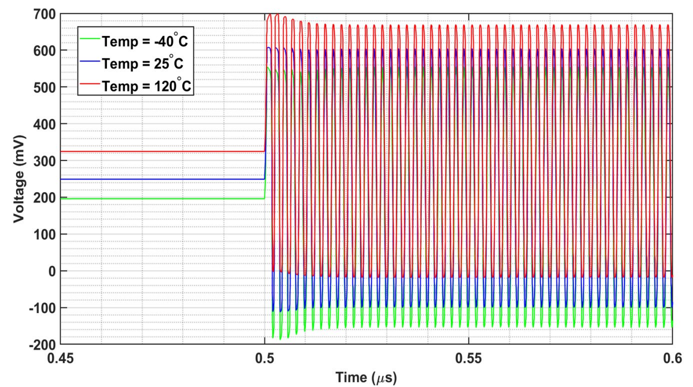


Fig. 14. Influence of thermal stress on the $S\&H$ voltage sensor attenuator for an input sine wave of 500 MHz.

were 30 mV higher and 80 mV lower compared to that of the nominal temperature, at −40 °C and 120 °C, respectively. Further simulations were performed on the voltage sensor to analyze how thermal stress caused variation in the output voltage in steady state conditions. It was found that the output DC offset of the voltage sensor varied with temperature only by ±150 mV for input frequencies lower than 550 MHz.

Moreover, it was verified in Cadence Virtuoso that the input attenuator was the root cause for the DC offset. Fig. 14 shows the simulated output response of the DC attenuator when subjected to a sine wave input signal of 500 MHz frequency and 1 V peak voltage at nominal and extreme temperatures. It can be observed that thermal stress causes only a DC offset (±65 mV) and there is no observable change in the peak output voltage. Furthermore, it was found out that for input frequencies above 550 MHz, the peak output voltage was reduced at 120 °C. This is due to the filtering effect of the compensation capacitors. Since conducted emission tests were performed at much lower frequencies, thermal stress did not affect the peak output voltage of the sensor. Although there exists a DC offset due to temperature variation, it was checked that the reduction of the output peak-to-peak voltage levels of the sensor at maximum temperature was due to decreased internal peak-to-peak current levels of the $H$-clock tree.

To sum up, in this case study, the PDN of the ICEM model is not influenced by HAST aging. However, thermal stress does have an impact on the PDN, causing deviations in its lumped passive elements. The IA block of the ICEM model is influenced by both aging and thermal stress, due to different physical mechanisms, though. Aging reduces the IA amplitude, and the conducted emission levels demonstrate an inverse variation with temperature. Since the IC under test is custom-designed in SOI technology, the developed ICEM-CE model cannot be compared directly with other ICs. The main difference from standardized models is the inclusion of HAST aging and thermal stress in the parameters of the proposed model.

## IV. Conducted Immunity Results and Discussion

This section deals with the conducted immunity analysis of two independent analog blocks, i.e., *S-R* latch and 3-stage CSVCO integrated into the tested IC. The extraction of two separate PDNs via $S$-parameter measurements and IB blocks through the DPI look-up table technique are explained. Moreover, the effects of HAST aging and thermal stress at −40 °C and 120 °C are analyzed in measurements and incorporated in the ICIM-CI model.

The DPI measurement setup mentioned in Section II-E was used to evaluate the susceptibility profiles of each tested circuit. The incident power was varied from 1 dBm to 30 dBm with a step size of 1 dBm while the frequency was changed from 1 MHz to 1 GHz in 10 MHz steps. For both tested structures, the continuous wave EM disturbance was superimposed over a 5 V DC bias only into its isolated power supply. The failure criterion considered for the *S-R* latch was ±10% of the DC offset with a dwell time of 1 second. Similarly, the ±10% changes in frequency or in the peak-to-peak voltage of the CSVCO were considered as its DPI failure criteria. All selected tolerance limits were similar to industry standards. Moreover, a dwell time of 3 seconds was set for the latter in order to allow it enough time to stabilize after each power/frequency increment.

### A. Influence of Aging on Conducted Immunity

As highlighted in Section I, the PDN blocks of the ICIM-CI and the ICEM-CE are identical and were extracted from $S$-parameter measurements. Hence, the same notation as the ICEM-CE schematic were re-used for the impedance pro-

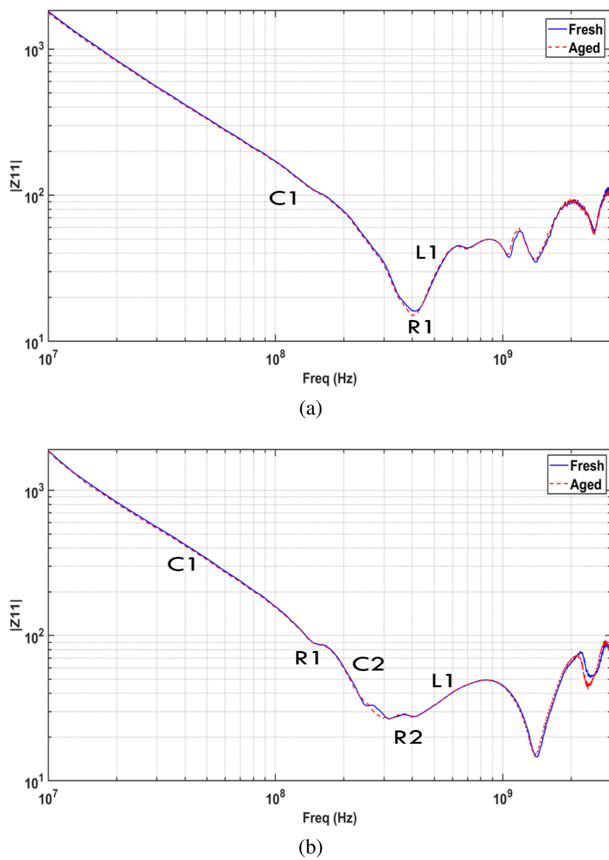


Fig. 15. Impact of aging on measured impedance profile of V$_{DDI}$ of: (a) analog *S-R* latch; (b) 3-stage CSVCO.

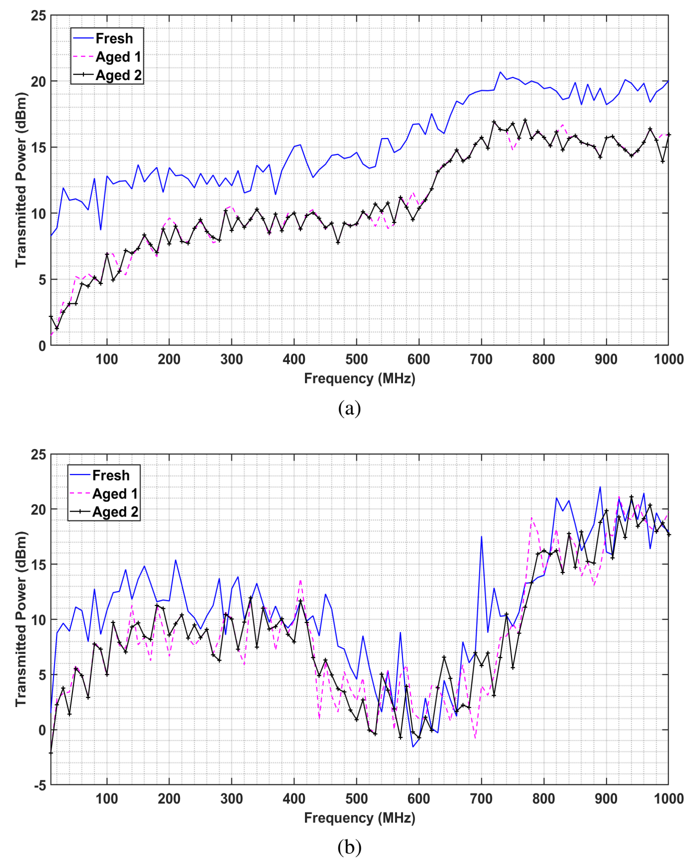


Fig. 16. Effect of aging on DPI profile of: (a) analog *S-R* latch; (b) 3-stage CSVCO.

files of the tested immunity circuits. Two independent $Z_{11}$ impedance profiles of the V$_{DDI}$ of the analog *S-R* latch and the 3-stage CSVCO are shown in Fig. 15a and 15b, respectively. Even though both circuits have identical pads their impedance profiles are entirely different. The reason for this is due to the distinct mutual coupling, since the V$_{DDI}$ pad of the *S-R* latch is closer to its G$_{NDI}$ pad compared to the CSVCO. No parasitic resonance was observed in Fig. 15a, therefore R2 and C2 are non-existent in the PDN of the *S-R* latch compared to the CSVCO. Similar to the $Z_{11}$ profile of the $H$-clock tree, the impedance profiles of both immunity test circuits were not impacted by aging.

The IB block of the ICIM-CI model was constructed using look-up tables which correspond to the amount of transmitted power in the IC pin that can cause its malfunction. This can be extracted using DPI measurements. The transmitted power ($P_t$) is measured by the power meter, and corresponds to the power injected at the PCB input. It depends on the input pin impedance and can also be calculated using $P_{inc} \times (1-|S_{11}|^2)$, where ($P_{inc}$) is the incident power. Hence, $P_t$ is the actual power that couples into the IC pin and is used to determine the conducted immunity profile.

To construct two separate IB blocks, DPI testing was performed by injecting conducted EM disturbances into the V$_{DDI}$ pins of the *S-R* latch and the CSVCO. The power $P_t$ to induce malfunction was determined using each circuit $S$-parameters. Fig. 16a shows the conducted immunity profile of the analog *S-R* latch. The failure criterion applied for the *S-R* latch was the DC-offset of the output signal monitored at the Q pin. The immunity profile for the fresh DUT shows a gradual increase in $P_t$ from 8 dBm at 1 MHz to 20 dBm at 1 GHz. This behavior demonstrates that the *S-R* latch is more susceptible at lower frequencies. Therefore, the combined effect of the package and the capacitance of the input pad results in filtering effects, hence attenuating power in higher frequency.

The frequency and the peak-to-peak voltage of integrated oscillators are important parameters to determine their stability. Thus, for DPI testing of the CSVCO, both parameters were considered as the failure criteria. The conducted immunity profile of the CSVCO is visible in Fig. 16b. The immunity behavior of the CSVCO is very different compared to the *S-R* latch. Overall, the package and input pad capacitance effect is demonstrated here as well, since the highest conducted immunity is observed above 850 MHz. However, the CSVCO is the most susceptible between 600 to 700 MHz. The reason for this could be due to the injected frequency being close to the operating frequency (703 MHz) of the CSVCO. As mentioned in Section II-C, the FD circuit is added at the output stage of the CSVCO in order to reduce the output frequency (62.5 MHz). Although the power supply of the FD is entirely isolated from EMI, it may still impact the conducted immunity evaluation. Since the CSVCO is a non-linear circuit, a small deviation in transistor characteristics due to aging may have a higher impact on the immunity profile (comparing Aged 1

and Aged 2 in Fig. 16b) than for a similar pseudo circuit as the S-R latch.

DPI testing was performed on several aged DUTs, at ambient temperature, having the same failure criteria for both tested blocks. In general, aging due to HAST induced a decrease in the conducted immunity levels of both tested circuits. The immunity profile waveforms remained the same with reduced immunity power levels. As seen in Fig. 16a, the average $P_t$ levels of the aged samples were 6 dB lower than the fresh sample within the tested frequency spectrum. Hence, aging only impacted the IB block of the ICIM-CI model of the *S-R* latch. The lower $P_t$ and corresponding frequency values were then updated in the IB look-up table to include the effect of aging in the ICIM model.

To verify the assertion that aging affects the IB block and lowers the $P_t$ levels that can trigger a failure, the conducted immunity of the CSVCO was compared with respect to aging (Fig. 16b). In this case, the aged $P_t$ levels were slightly reduced (4.5 dB), compared to the fresh version, in particular in frequencies below 200 MHz. At higher frequencies, the immunity levels of the fresh and aged samples were comparable. The degradation mechanisms (NBTI) occurring in the CSVCO and the *S-R* latch are not the same. Since both circuits have different functionalities and failure criteria, the impact of aging is distinct. However, it can be concluded that aging due to HAST reduces conducted immunity levels in a given frequency range for both tested analog blocks. These aged power levels can be updated in the IB block of each ICIM model to include the effect of aging. This may be achieved by the means of specified deviations on IB look-up tables, or different IBs according to the fresh/aged state of the block.

## *B. Influence of Thermal Stress on Conducted Immunity*

To validate the impact of thermal stress on the PDN of both the *S-R* latch and the CSVCO, $S$-parameter measurements were performed on fresh PCBs at extreme temperatures (−40 °C and 120 °C). As expected, the $Z_{11}$ profiles of the $V_{DDI}$ of the *S-R* latch (Fig. 17a) and the CSVCO (Fig. 17b) exhibited variations with thermal stress over the entire frequency range. Those deviations could not be neglected and all tolerances were involved in the PDN block of the individual ICIM-CI models of the *S-R* latch (Table IV) and the 3-stage CSVCO (Table V).

Thermal stress influences the MOSFET characteristics in ICs and can vary the robustness of an analog circuit. For the analog *S-R* latch the 5 V (25 °C) DC level of the output was increased to 5.3 V (−40 °C) and 4.7 V (120 °C) with temperature variations. Hence, it was considered that the $V_{th}$ levels of the MOSFETs in the latch were the root cause of the change in DC output levels. For the CSVCO, the operating frequency was verified in simulations to be inversely proportional to temperature. Its output frequency after the FD, was found to be 62.5 MHz at nominal temperature and varied to 68.3 MHz and 53.8 MHz at −40 °C and 120 °C, respectively. For the CSVCO, the shift in frequency meant that the $V_{th}$ and the $\mu_{eff}$ were influenced by temperature.

To validate the effect of thermal stress on the IB block, multiple fresh DUTs were subjected to DPI testing at nominal and extreme temperatures, by injecting into the $V_{DDI}$s of the *S-R* latch and the CSVCO. Similar failure criteria considered for the nominal temperature were applied at extreme temperatures for both circuits. The influence of thermal stress on the conducted immunity profiles of the *S-R* latch and the 3-stage CSVCO is illustrated in Fig. 18a and 18b, respectively. For the *S-R* latch, the increase in temperature lowered the conducted immunity $P_t$ levels. As observed in Fig. 18a, compared to the nominal temperature, the average $P_t$ levels were improved by

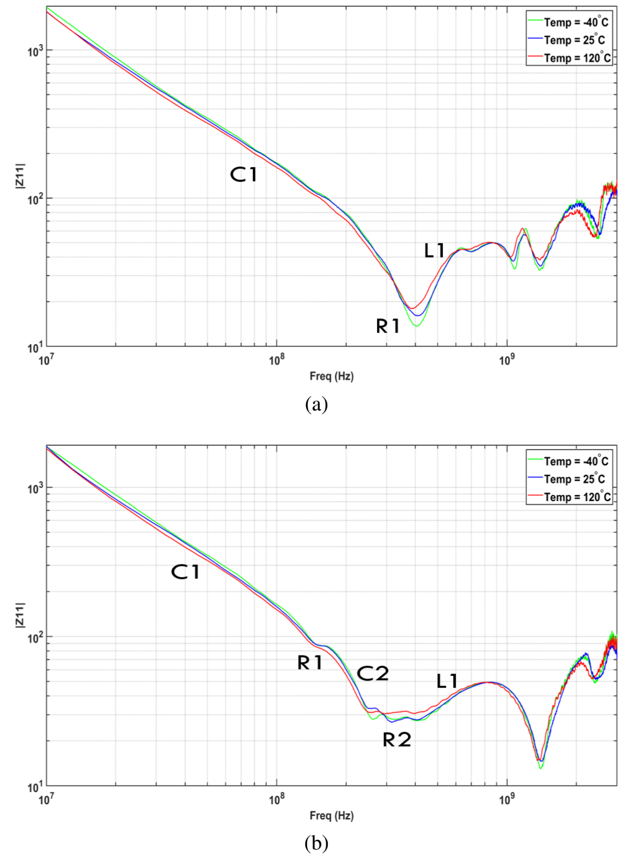


Fig. 17. Influence of thermal stress on measured impedance profile of $V_{DDI}$ of: (a) analog *S-R* latch; (b) 3-stage CSVCO.

TABLE IV
DEVIATIONS IN PDN PARAMETERS EXTRACTED AT THE $V_{DDI}$ OF THE ANALOG *S-R* LATCH DUE TO THERMAL STRESS

| Component | T = -40 °C | T = 25 °C | T = 120 °C |
|---|---|---|---|
| C1 | 8.6 pF | 9.2 pF | 10.1 pF |
| R1 | 15 Ω | 17 Ω | 19 Ω |
| L1 | 8.4 nH | 9.1 nH | 10 nH |

TABLE V
DEVIATIONS IN PDN PARAMETERS EXTRACTED AT THE $V_{DDI}$ OF THE 3-STAGE CSVCO DUE TO THERMAL STRESS

| Component | T = -40 °C | T = 25 °C | T = 120 °C |
|---|---|---|---|
| C1 | 8.8 pF | 9.6 pF | 10.6 pF |
| R1 | 87 Ω | 88 Ω | 89 Ω |
| C2 | 12.2 pF | 13.3 pF | 15 pF |
| R2 | 27 Ω | 28 Ω | 32 Ω |
| L1 | 9.2 nH | 10.6 nH | 11.9 nH |

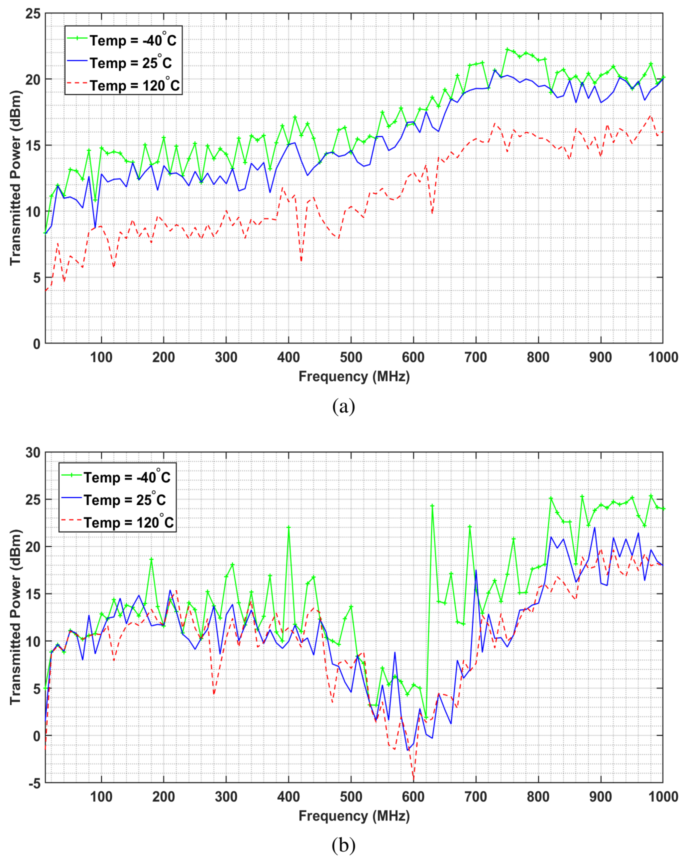


Fig. 18. Influence of thermal stress on DPI profile of: (a) analog *S-R* latch; (b) 3-stage CSVCO.

1.8 dB at minimum temperature while they were lowered by 5.1 dB at maximum temperature. Due to the drift in $V_{th}$ levels of the MOSFETs in the latch, the conducted immunity of the latter was extensively influenced by the thermal stress.

In the case of the CSVCO (Fig. 18b), the conducted immunity profile approximately remained the same at 120 °C across the entire frequency spectrum. However, at −40 °C, the average $P_t$ levels improved substantially by 9.2 dB between 600 to 700 MHz. It continued to be slightly higher (1 dB) than the $P_t$ levels at 25 °C for frequencies between 700 MHz to 1 GHz. The conducted immunity of the CSVCO was found to be resilient to higher temperatures, however, lower temperatures had an impact on its conducted immunity due to the drift in $\mu_{eff}$ and $V_{th}$ levels. Hence, for both circuits, the thermal stress influenced their respective IB blocks of the ICIM-CI models. Similarly to aging, deviations can be applied to the IB look-up tables as a function of temperature.

To summarize, the PDN blocks of the two tested circuits, i.e. *S-R* latch and CSVCO, were shown to be influenced by thermal stress rather than aging. It was also verified that HAST aging lowers the immunity power levels of each circuit's IB block for a specific frequency range. Intrinsic degradation mechanisms such as NBTI are the cause of that behavior. Further, the conducted immunity levels of the *S-R* latch were demonstrated to inversely vary with thermal stress, while the CSVCO's immunity was impacted only at lower temperatures. The reason is due to thermal stress causing a drift in $\mu_{eff}$ and $V_{th}$ levels of the latter. Further explanation of the influence of temperature on physical transistor parameters i.e. $V_{th}$ and $\mu_{eff}$, as well as their relation to the EMC behavior of the integrated blocks can be found in [50].

## V. Conclusion

The concept of involving environmental effects such as aging and thermal stress on the conventional conducted emission (ICEM-CE) and immunity (ICIM-CI) models was put into practice herein through measurements and transistor level simulations. HAST testing was performed for the first time on a custom-designed IC developed in SOI technology, comprising several independent analog CMOS structures such as $H$-clock tree, *S&H* voltage sensor, *S-R* latch, and 3-stage CSVCO, to characterize the effect of aging on conducted emission and immunity levels. It considered the combined effect of environmental stresses i.e., temperature and humidity that caused deviations in IC parameters. Further, extreme temperature tests were performed on several packaged ICs in order to extensively analyze the influence thermal stress on the conducted susceptibility and emission levels.

Unlike with HAST aging, the PDN block of the developed models was influenced by thermal stress causing variations in its lumped passive elements, which must be included in the models for improved accuracy. However, HAST aging caused the permanent degradation mechanism (NBTI), while thermal stress temporarily impacted the MOSFET characteristics (i.e., $\mu_{eff}$ and $V_{th}$) that could cause IC soft failures. Those mechanisms were demonstrated to almost exclusively influence the active blocks (i.e., IA and IB) of the conducted emission and immunity models.

A simulation-based transistor-level approach was used to develop the IA block of the ICEM-CE model, providing a good correlation with measurements. By applying conducted emission measurements using the 1- Ω method on the $H$-clock tree, it was demonstrated that the external current emission levels would degrade with aging and temperature increase. This effect was traced back to the variation in the internal current (IA) in case of thermal stress. Therefore, it was shown that constant proportionality coefficients extracted from simulations (temperature) and measurements (aging) could be included into the IA blocks of the models.

Using DPI measurements on two independent *S-R* latch and CSVCO analog circuits, it was shown that aging due to HAST increases the conducted susceptibility levels as a function of frequency depending on the functionality of the analog block. Moreover, high temperature stress was found to also reduce their conducted immunity levels depending on the drifts in $V_{th}$ and $\mu_{eff}$ levels. Specified deviations in the look-up tables can be applied to include the influence of aging and thermal stress on the IB block.

For the considered scenarios, the developed ICEM-CE and ICIM-CI models were demonstrated to quantify conducted emission and immunity levels with enough accuracy under aging and thermal stress. This paves the way to the inclusion of such deviations in future revised versions of those standards.

## ACKNOWLEDGEMENT

This publication reflects only the authors' view, exempting the European Union from any liability. Project website: http://etn-peter.eu/.

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