Influence of Temperature on the EFT Immunity of Multi-Stage Integrated Oscillators

Qazi Mashaal Khan, *Graduate Student Member, IEEE*, Mohsen Koohestani, *Senior Member, IEEE*, and Richard Perdriau, *Senior Member, IEEE*

***Abstract*—The reliable operation of an integrated circuit (IC) can be affected by transient electromagnetic disturbances and temperature variations. In this paper, the performance of three oscillator circuits, namely 3- and 5-stage current-starved voltage controlled oscillators and a 3-stage ring oscillator, is compared with respect to electrical fast transients (EFT) under the influence of thermal stress. The main objective is to compare and assess, by means of measurements, the EFT immunities of integrated oscillators with the same electrostatic discharge (ESD) protections but different circuit topologies. The failure modes caused by EFT are proposed based on the considered failure criterion, i.e. the output frequency of the oscillator. Moreover, the importance of the IC package on the immunity levels of each oscillator is investigated. Additionally, the output frequency response of each oscillator to the combined EFT and temperature stresses is analyzed without the external parasitic effects. The results show that the 5-stage CSVCO is the most resilient oscillator to temperature variations, whereas it is the least immune to the combined effect of EFT and temperature. Moreover, a distinct behavior in each tested oscillator's frequency is observed for the in-phase EFT injections due to the topology of the circuit. Relevant MOSFET characteristics such as on-state drain-to-source resistance, drain currents, power dissipation, effective mobility and threshold voltage level are further analyzed under the influence of thermal stress and EFT disturbances. The root cause of higher EFT susceptibility of the 5-stage CSVCO is found to be the considerable variation of the on-state resistance due to the combined reduction of effective mobility and absolute threshold voltage levels of the MOSFETs. As a result, the power dissipation rises and causes thermal runaway.**

***Index Terms*—IC, EFT, ESD devices, temperature variation.**

I. Introduction

WHILE electromagnetic (EM) immunity problems may be caused by a variety of mechanisms, the main point of failure in a modern digital device can often be an integrated circuit (IC) [1]. Due to the downscaling of CMOS transistors, a modern IC can be sensitive to the electrostatic discharge (ESD) stress, which leads to the reduction of its intrinsic robustness [2]. Therefore, all supply and input/output (I/O) pads of an IC include ESD protection circuits. Transient conducted immunity testing such as electrical fast transients (EFT), as defined in IEC 61000-4-4 [3], is typically performed in industry to check the robustness of ESD devices [4].

EFT induced transients act as an exponential voltage pulse, in contrast to the underdamped sinusoidal voltage waveforms generated in system-level ESD tests [5]. The EFT signal, consisting of a series of bursts, can be injected into the power supply or functional pins of an IC through magnetic or electric coupling. This can interfere with the functional behavior of the IC, causing for example a transient induced latch-up effect or even irreversible damage [6].

Integrated oscillators are a vital part of analog/digital IC blocks such as phase-locked loops and are vulnerable to transient EM disturbances, even if protected by ESD devices [7]. Temperature variations can also influence the protection capability of the ESD devices, hence, affecting the immunity of the oscillator. Additionally, faster transistor switching in the oscillator's inverter stages can raise junction temperatures and diminish its performance [8]. Therefore, stability against temperature changes and immunity to transient EM disturbances, such as EFT, require reasonable attention to ensure reliable operation of an integrated oscillator.

In literature, researchers have focused on analyzing and improving the latch-up immunity of CMOS ESD devices [9], [10]. In addition, some authors have specifically studied the latch-up behavior of ESD circuits under EFT stress [11]. The importance of analytical EFT modelling to investigate the immunity of an IC has been discussed in [12]–[14]. Furthermore, the characterization and prediction of EFT immunity through numerical simulations have been highlighted in [15]–[17]. The susceptibility to conducted EM disturbances (continuous wave and transient) in the power supply of ring oscillators has been analyzed in [18], [19]. Moreover, some work has been performed to observe the effect of temperature variations on the behavior of ESD devices in an IC [20]–[22]. To the best of the authors' knowledge, the comparison of EFT immunities of integrated oscillators, having the same ESD protection devices but different topologies, has not been investigated. Moreover, the influence of temperature on such immunities has not yet been addressed.

In the current study, the EFT immunity of multi-stage current starved voltage controlled oscillators (CSVCO) and

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(*Corresponding author: Qazi Mashaal Khan.*)
Q. M. Khan is with the ESEO School of Engineering, Department of Electrical and Electronic Engineering, 49107 Angers, France, and also with the Institut National des Sciences Appliquées, Department of Electronics Engineering, 35708 Rennes, France (email: qazimashaal.khan@eseo.fr)
M. Koohestani and R. Perdriau are with the ESEO School of Engineering, Department of Electrical and Electronic Engineering, 49107 Angers, France, and also with the Institute of Electronics and Telecommunications of Rennes, University of Rennes 1, 35042 Rennes, France (mohsen.koohestani@eseo.fr; richard.perdriau@eseo.fr).
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a ring oscillator (RO) is compared and analyzed at ambient and extreme temperatures through measurements. The effect of the IC package on the observed EFT immunity levels of each oscillator is also investigated. Furthermore, simulations at transistor level are implemented to identify the change in oscillator frequency due to EFT injection and analyze the effect of EFT and thermal stress on relevant MOSFET characteristics.

The paper is organized as follows. Section II describes the custom designed IC including the ESD protection circuits and printed circuit board (PCB), as well as comparing the robustness of each oscillator to temperature variation. This section also describes the EFT simulation and hardware test setup, along with the specification of the observed failure modes. Section III presents the experimental results of the EFT immunity of all integrated oscillators at nominal and extreme temperatures. Section IV includes the simulation based frequency response of each oscillator (with and without external parasitics) due to EFT under the influence of thermal stress. Moreover, relevant MOSFET characteristics are also analyzed through simulation when subjected to EFT and thermal stress. Finally, the conclusions of this study are presented in Section V.

II. Materials and Methods

This section introduces the IC and PCB designed for this study. Then, a pre-stage study is conducted on the effect of temperature on oscillators' frequency, in order to better define the immunity criterion for EFT. It is followed by the simulation setup used to generate and inject the EFT signal into the supply rail of the tested oscillators. The experimental test setup to characterize the transient immunity of the integrated oscillators under thermal stress is also described.

A. IC and PCB Design Description

For the purpose of the study three conventional oscillators, a 3- and 5-stage CSVCO and a 3-stage RO were chosen (Fig. 1). They were integrated, among other structures, into the 1.52 mm × 1.52 mm PETER_ESEO research die [23], which was fabricated in silicon-on-insulator (SOI) CMOS 180 nm 5 V technology. They were designed to have matching aspect ratios and generate sinusoidal signals with stable output frequencies. The design and layout of the oscillator circuits was conducted using Cadence Virtuoso.

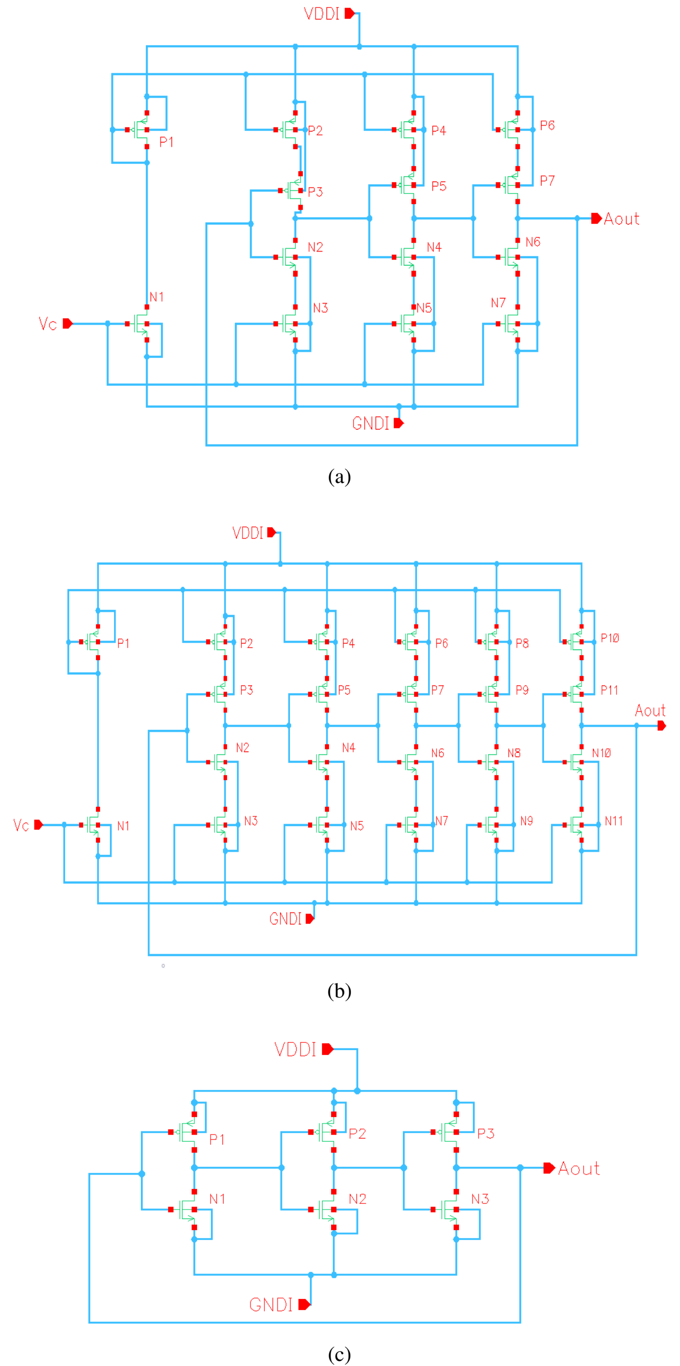


Fig. 1. Schematic of the multistage integrated oscillators: (a) 3-stage CSVCO; (b) 5-stage CSVCO; (c) 3-stage RO.

The die is surrounded by a 52-pad ring with N-MOS based ESD protection devices to both the global power supply rail (V_{DDO}) and ground. The V_{DDO}, V_{DDR} and V_{DD5} pins power up the padring and the digital blocks with reduced noise coupling. Likewise, the G_{NDO} and G_{NDR} pins are ground references for the padring and the digital blocks, respectively. Each oscillator has an isolated power supply pad (V_{DDI}) and a single separate ground (G_{NDI}), due to the use of SOI technology (Fig. 1. The output of each oscillator is connected to an analog pad having a parasitic capacitance, and an ESD protection circuit which will clamp the generated signals that are not within the 0 to 5.5 V range. The internal ESD circuits of the V_{DDI}/G_{NDI} and analog I/O pads include N-MOS transistors with gate to source resistors to reduce the overall gate leakage current. In case of the analog I/O pad, a resistor is also included in series between the pad and the internal rail.

The die samples were packaged in a 64-pin ceramic quad flat package (CQFP). All power supply and ground pads were bonded to the package pins with spacing in between to minimize the effect of mutual inductive coupling. This makes it possible to not only inject more power into the supply pads but also monitor high frequency signals.

The primary difference in oscillator topologies is that the CSVCO has externally biased MOSFETs that control the

current provided to its inverter stage. The biasing supply (V_C) is connected to those MOSFETs to reduce the output power and control the frequency range [24]. Contrarily, for the RO, the output frequency only depends on the inverter cell stages and the voltage supply. A buffer is included at the output stage of the RO to stabilize the amplitude of the generated signal.

A multi-stage digital frequency divider (FD) circuit is added at the output stage of each oscillator to decrease the fundamental frequency of the generated signal [25]. The FD is powered by V_{DD}, which is isolated from each oscillator's individual power supply and enables monitoring the frequency at the analog output pad without filtering effects caused by the parasitic pad capacitance. The simulated maximum operating clock frequency of the FD was found to be 900 MHz.

To test the conducted immunity of the IC, two similar 13 cm × 13 cm 4-layer FR4 PCBs, referred to as packaged and chip-on-board (COB), were designed according to IEC 62132-4 [26] using Altium Designer. The former PCB variant consisted of the CQFP package, while in the latter version the die was mounted directly on the PCB using a conductive epoxy resin (LOCTITE ECCOBOND EO1016). It was confirmed that the PCBs were not overloaded with non-linear components, to precisely measure the immunity of the IC. For both versions, all isolated grounds of the IC were connected to the global ground. Additionally, a 470 Ω resistor was added in series to the output of each tested oscillator, in order to limit high voltage signals from being re-injected into the IC or the oscilloscope [27].

B. Pre-Stage Study: Effect of Temperature on the Output Frequency of the Integrated Oscillators

Deviations in temperature can progressively impact the performance of CMOS circuits such as oscillators. It can effect the drain current, effective mobility (μ_{eff}) and the threshold voltage (V_{th}) of the CMOS transistors in the oscillator inverter stage [28]. The packaged PCB variant was placed in a SATIMO thermal oven with voltage biasing applied through high temperature cables (Amphenol-RF 095-902-466-004). While maintaining the ambient temperature at 25 °C, the output frequency of each oscillator at the output pin was monitored through an oscilloscope with 1 MΩ input impedance. To verify the dependency of the output frequency on temperature, the former was recorded at extreme temperatures (−40 °C and 120 °C) for all tested oscillators as shown in Table I. Although the operating and output frequencies of each oscillator are different, the gate size in the inverter stage is identical for all oscillators for a fair comparison. Hence, the temperature variation will equally affect on the transistors' V_{th} levels. Moreover, the respective minimum and maximum temperatures were chosen since it corresponds to the temperature limits of all the components soldered on the tested PCB.

For all oscillators, the output frequency was found to be inversely proportional to temperature (Table I), which is due to altering the μ_{eff} and drain currents of the MOSFETs in the inverter stages as a function of frequency. For the FD circuit, temperature changes only affected the DC offset (±0.2 V) of the output voltage and not the frequency. However, with the rise in temperature, for input frequency signals greater than 900 MHz, the propagation delay in the FD becomes higher than the oscillator's period, and the measured output frequency is thus considerably reduced.

TABLE I
MEASURED OPERATING (BEFORE FD) AND OUTPUT FREQUENCIES (AFTER FD) AT NOMINAL AND EXTREME TEMPERATURES

Type of Oscillator	Operating frequency	Output frequency (−40 °C)	Output frequency (25 °C)	Output frequency (120 °C)
3CSVCO	703 MHz	68.3 MHz	62.5 MHz	53.8 MHz
5CSVCO	271 MHz	71.6 MHz	66.1 MHz	61.4 MHz
3RO	955 MHz	117.4 MHz	97.7 MHz	78.2 MHz

It was found that the deviations of output frequency from the nominal frequency for the 3- and 5-stage CSVCO and 3-stage RO over the entire temperature range were +9.3%, +8.3%, +20.2% (at −40 °C), and −13.9%, −7.1%, −19.9% (at 120 °C), respectively. Comparing the 3-stage CSVCO and RO, the former has a higher on-state drain-to-source resistance in the inverter stage (5.8 kΩ compared to 1.6 kΩ at the ambient temperature) due to the inclusion of the biasing transistors. That reduces the drain current in the CSVCO inverter stage resulting in a lower frequency deviation with thermal stress.

As far as the RO is concerned, the FD circuit was found to have an impact on the observed output frequency at extreme temperatures due to the operating frequency (955 MHz) being higher than the maximum clock frequency (900 MHz). For the CSVCO, the increase in the number of stages from 3 to 5 improved the resilience of the output frequency to temperature variations (Table I) due to a higher number of stages. In fact, due to the external biasing voltage being different for both CSVCOs (1.8 V and 1.6 V for 3- and 5-stage CSVCOs), the $V_{GS} - V_{th}$ term, to which the drain current is proportional, does not vary over temperature in the same proportion for both CSVCOs.

C. EFT Simulation Setup

EFT is a low energy test having a wide spectral frequency content creating problems in sensitive analog circuits such as integrated oscillators. In this paper, EFT is only injected into the V_{DDI} of each oscillator. The equivalent circuit for the EFT transient noise generator (Fig. 2a) defined in IEC-61000-4-4 [3], was simulated in Cadence Virtuoso. Only the impedance-matching resistor R3 (50 Ω) and the DC-blocking capacitor C2 (10 nF) are fixed by the standard. The charging resistor R1 and the capacitor C1, used to store the charging energy, were set to 5 Ω and 6 μF. The resistor R2 (12 mΩ) was used to shape the pulse duration of the EFT signal. According to [3], each individual pulse was characterized by a 5 ns rise time, 50 ns pulse width, 100 kHz spike frequency, 0.75 ms burst duration and 300 ms burst repetition. The positive polarity EFT signal is ramped from 250 V to 2 kV.

As seen from Fig. 2a, the EFT signal input path includes the generator circuit, the biasing power supply V3 (5 V) in

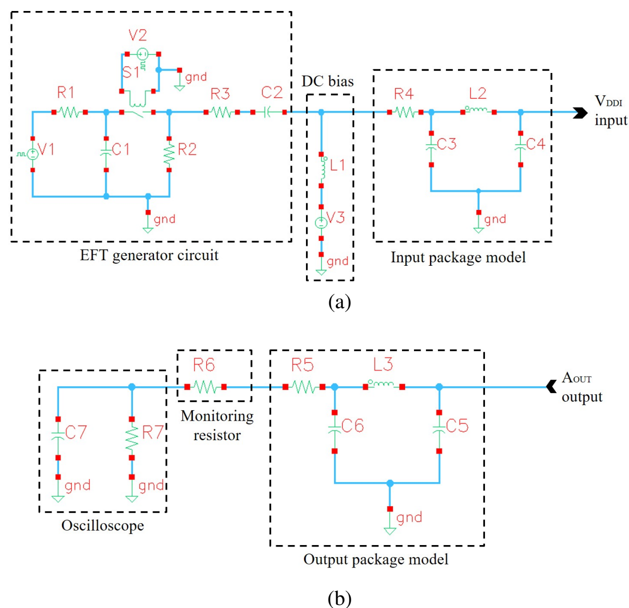


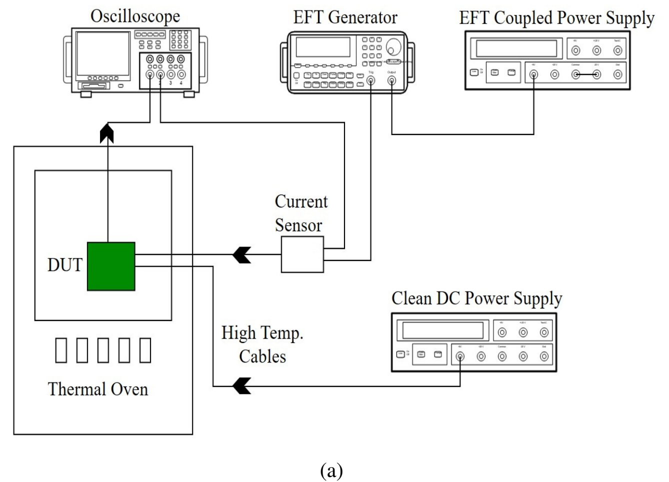
Fig. 2. EFT simulation setup for the packaged version: (a) input path; (b) output path.

series with a choke inductor L1 (100 μH), and the IC package model feeding the V_{DDI} pad of the oscillator. The inductor ensures that a high impedance path is created for the EFT disturbances so that they are not absorbed by the supply. The output path is composed of the analog output pad (A_{OUT}), the output package model, monitoring resistor and the oscilloscope model (Fig. 2b). The monitoring resistor R6 (470 Ω) has a temperature coefficient of 100 ppm/°C. The oscilloscope model includes a high impedance resistor R7 (1 MΩ) and its parasitic capacitance C7 (16 pF) which only affects the peak voltage of the oscillating output signal.

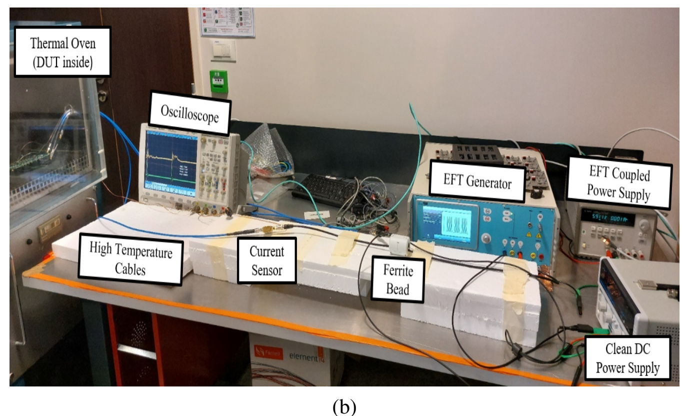
The CQFP package of the chip was modelled using the IC-EMC software [29], to extract the approximated package model consisting of passive lumped elements found through IC parameters such as die size, pitch, lead frame and cavity sizes. The I/O package model elements are R5 (4.5 Ω), C6 (10.2 pF), L3 (9.1 nH) and C5 (1.7 pF). The simulation setup will be used in Section IV to analyze the effect of the EFT signal on the frequency behavior as well as relevant MOSFET characteristics of the considered oscillators at extreme temperatures.

D. EFT Measurement Test Setup

The test bench includes an EFT generator (EMC-Partner IMU4000), two dual-channel DC power supplies (Agilent E3631A), a pulse current sensor (HPPI CS-0V5-A), an oscilloscope (Agilent MSO7104A), and the SATIMO oven. The EFT measurement block diagram and the test setup are depicted in Fig. 3a and 3b, respectively. One of the power supplies is connected to the internal coupler of the EFT generator, making it possible to superimpose the disturbance with the DC voltage (5 V) feeding the V_{DDI} pin of each oscillator. The channels of the other power supply are connected to the V_{DD} and V_C of the DUT providing a constant voltage of 5 V and 1.8 V, respectively. The V_{DD} is the global power supply that



(a)



(b)

Fig. 3. EFT measurement: (a) block diagram; (b) test setup.

powers up the padring and the FD circuit. Both V_{DD} and V_C are completely isolated from the injected EFT disturbances.

The current sensor, with a nominal sensitivity of 0.5 V/A, is connected in series with the EFT generator to monitor the input current being injected into the device under test (DUT). A ferrite bead is also connected to the EFT generator cable to filter out high frequency RF signals being re-injected into the power supply. The DUT is placed inside the oven and the output pin of the tested oscillator is connected to one of the channels of the oscilloscope (1 MΩ) via high temperature cables. The second channel of the oscilloscope is connected to the current sensor's 50 Ω monitoring output.

E. EFT Failure Criterion and Modes

The operating frequency of an oscillator is typically used to evaluate its susceptibility to continuous wave EM disturbances and can also be considered to characterize its transient immunity. In this paper, the failure criterion is a ±10% deviation from the nominal output frequencies of the multi-stage CSVCO and RO at ambient and extreme temperatures. EFT failure modes, previously defined in [30] for microcontrollers, are redefined here to evaluate the EFT immunity of the integrated oscillators. The apparent failure types classified from A to E are the following:

- **A-type**: no failure occurs, and the frequency of the oscillator remains within the defined tolerance limit.

- **B-type**: the oscillator's frequency exceeds the tolerance limit but self-recovers to its nominal frequency as soon as EFT is removed.
- **C-type**: this soft failure usually occurs in microcontrollers when the state machine crashes into an unknown state due to EFT disturbance and can only be recovered by an external reset of the core. This type of failure is not applicable for purely analog devices such as oscillators.
- **D-type**: the oscillator's frequency goes beyond the tolerance limit and only recovers to its nominal frequency after EFT is removed and power cycling is performed.
- **E-type**: the oscillator's frequency crosses the tolerance limit and never recovers to its original frequency even with power cycling.

III. Experimental Results and Discussion

This section deals with the comparison of measured EFT immunities of multi-stage CSVCOs and RO with and without the IC package. Furthermore, the effect of EFT immunity levels (positive and negative polarity) are compared at extreme temperatures. The positive and negative polarity EFT voltages were ramped from 250 V to 2 kV and −250 V to −2 kV in 20 V steps, respectively. A dwell time of 15 s was given at each EFT level in order to acquire the output voltage and input current of each oscillator at −40 °C, 25 °C, and 120 °C. The test was terminated when an E-type failure occurred and the oscillator was permanently damaged. Due to the use of isolated power supplies, an E-type failure only damaged the supply pad of the tested oscillator, leaving the other supply oscillator pads unaffected. Additionally, A-type failures were never observed in any case, since even at the minimum applied EFT voltage (250 V or −250 V), all oscillators were operating beyond the tolerance limits. Hence, most cases resulted in B-type failures. All EFT immunity level measurements were reproducible with other samples.

A. EFT Immunity Analysis at Nominal Temperature: Packaged vs. COB

To start with, positive polarity EFT disturbances were applied to packaged and COB versions of the oscillators at 25 °C. As an example, the output response and the injected EFT current for the 5-stage CSVCO are displayed in Fig. 4a and 4b, respectively. The response is shown for a 18 μs duration displaying two consecutive peaks of EFT injection (600 V). It should be noted that the steady-state oscillating output voltage of the 5-stage CSVCO was found to have a peak-to-peak voltage, DC-offset, and frequency of 232 mV, 1.17 V, and 66.1 MHz, respectively. It was observed that since the pulse width of each EFT spike was only 50 ns, the ESD protections were triggered after some delay, allowing the EFT voltage to be re-injected to the output. The latch-up effect of the ESD structures can be seen between the two consecutive EFT spikes, limiting the output voltage between 0 and 5.5 V and eventually stabilizing. That effect had a random final output level (clamped to either 0 or 5.5 V) for each EFT injection (75 peaks in each burst) and showed a damped oscillation due to the resonance between the output pad capacitance and

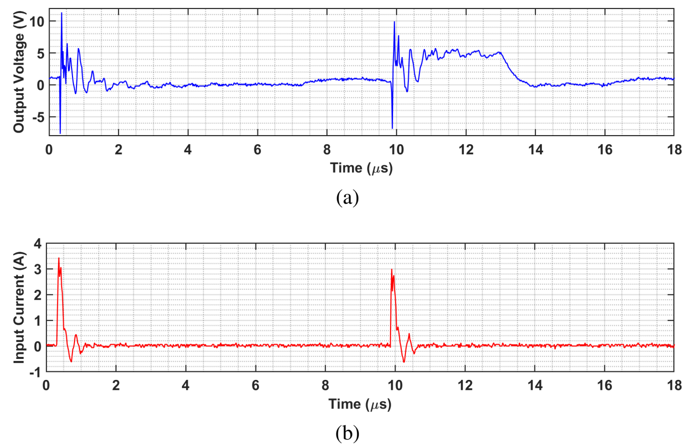


Fig. 4. Measured output voltage (a) and input current (b) for the 5-stage CSVCO at EFT = 600 V.

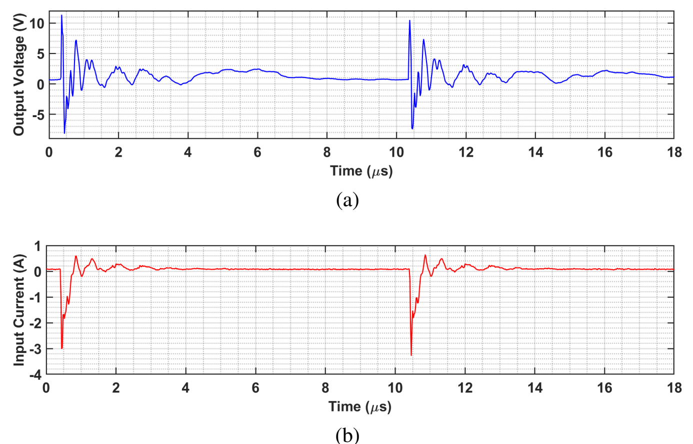


Fig. 5. Measured output voltage (a) and input current (b) for the 5-stage CSVCO at EFT = −600 V.

the bonding/package parasitics. As expected, it can be noticed that the pseudo period of that oscillation is higher for the packaged version in comparison to the COB, due to the added package inductance. In case of the injected EFT input current, all waveforms were repeatable.

Similarly, a negative polarity EFT voltage of −600 V was injected into the V_{DDI} pin of the 5-stage CSVCO while operating in steady state. The output response and the injected EFT current of the latter are shown in Fig. 5a and 5b, respectively. The output voltage response was comparable to the positive polarity EFT test, since the V_{DDI} pad includes identical N-MOS based ESD protections to both the supply rail and ground. The latch-up effect of the ESD structures remains entirely random and the output voltage eventually stabilizes. The observed input current was inverted, with its absolute peak-to-peak value similar to that of the positive polarity EFT current.

Fig. 6 shows the positive EFT immunity levels, with their specific failure modes, of all tested oscillators for packaged and COB ICs at ambient temperature. When comparing the packaged 3- and 5-stage CSVCOs, the latter was found to be more immune with an E-type failure detected at 830 V. In both CSVCOs, the output was able to self recover before eventually being damaged at their maximum bearable EFT

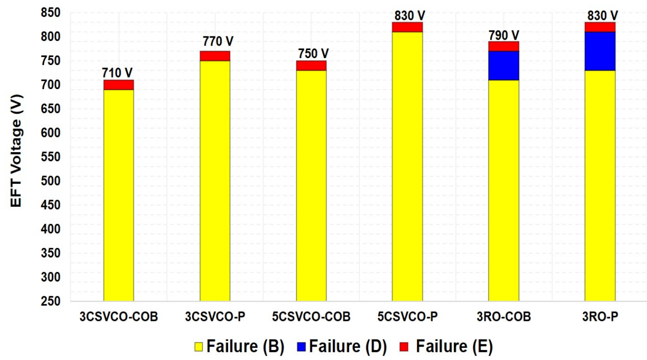


Fig. 6. Positive polarity EFT immunity of multistage CSVCO and RO at ambient temperature: packaged vs. COB.

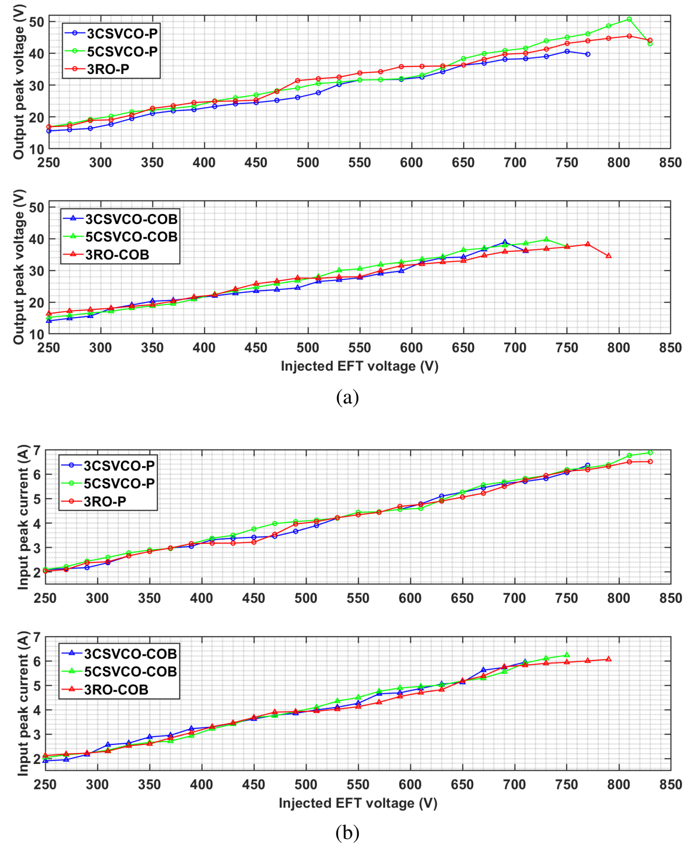


Fig. 7. Effect of EFT disturbances on multi-stage CSVCO and RO (packaged vs. COB) at ambient temperature: (a) output peak voltage; (b) input peak current.

voltage. Contrarily, in the packaged 3-stage RO, D-type failure started to occur at 730 V, before eventually turning to E-type at 830 V. The EFT immunity level of the 3-stage RO was found to be higher compared to the 3-stage CSVCO.

When analyzing the positive EFT immunity levels for the tested COB oscillators, all levels were reduced compared to the packaged ones. This was due to the package parasitics attenuating the injected EFT voltage and current going into the V_{DDI} pad of each oscillator. Moreover, the behavior of the oscillators to EFT and their respective failure modes were unaffected by the package. The 5-stage CSVCO was still more immune (750 V) than the 3-stage CSVCO (710 V). D-type was observed (similar to the packaged version) only for the RO at 670 V, ultimately becoming E-type at 790 V. The D-type failure effects in the RO for both packaged and COB may be due to the FD circuit being sensitive to EFT at its input above its maximum clock frequency (900 MHz) and locking up in a stable state, thus resulting in re-injection of the EFT voltage to the global power supply which was observed in simulations and measurements. Similarly to the packaged version, the 3-stage CSVCO EFT immunity was lower than the RO.

The output peak voltage and input peak current of each oscillator (packaged and COB) were further analyzed and are shown in Fig. 7a and 7b, respectively. As it can be observed in Fig. 7a the output peak voltage increases with the rise in EFT voltage in all the considered cases. Conversely, a drop in the output peak voltage can be observed when an E-type failure occurs. The output peak voltages for increasing EFT injected voltage were greater for the packaged IC than for the COB. The highest output peak voltage was observed for the 5-stage CSVCO, close to its maximum EFT immunity level, for both packaged (51.2 V) and COB (40.3 V) cases.

As indicated in Fig. 7b, the injected input current was also proportional to the increase in the applied EFT voltage for all tests at 25 °C. Similarly to the output voltage, the input peak currents for the packaged oscillators were slightly higher than the COB. Moreover, the largest peak input current was noted for the 5-stage CSVCO, near its maximum EFT immunity level for both with (6.9 A) and without (6.1 A) the package. Thus, the 5-stage CSVCO can withstand more injected EFT peak current than the remaining oscillators.

B. EFT Immunity Analysis of Integrated Oscillators at Extreme Temperatures

In Section II-B, it was demonstrated that the output frequency of all oscillators was inversely proportional to the rise in temperature, whereas the frequency of the 5-stage CSVCO was more resilient to temperature changes compared to the remaining oscillators. In this section, the positive and negative polarity EFT immunity of all the packaged oscillators are characterized including the effect of temperature variation.

The positive polarity EFT immunity levels of the packaged oscillators at extreme temperatures are displayed in Fig. 8. It was found that the immunity levels of all oscillators had reduced at 120 °C and improved at −40 °C, compared to the ambient temperature. Since all integrated oscillators have the same ESD protection devices, the temperature variation is affecting the performance of the latter. The temperature increase during the EFT stress reduces the ESD devices' protection capability, triggering current and holding voltages, hence reducing the overall transient immunity levels of each oscillator.

When comparing the 3- and 5-stage CSVCOs, the former had a better EFT immunity at −40 °C (1.1 kV) and at 120 °C (710 V). Even though the output frequency of the 5-stage CSVCO was found to be more resilient to temperature variations, its immunity to EFT disturbances was reduced at higher temperatures. This could be due to the reduction of the

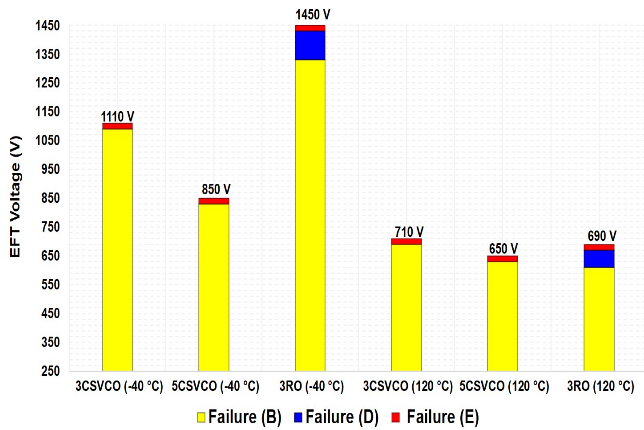


Fig. 8. Positive polarity EFT immunity of multi-stage CSVCO and RO (packaged) at extreme temperatures.

V_{th} levels of the higher number of biasing transistors due to temperature, resulting in lower levels of EFT immunity.

The RO was found to be the most immune at −40 °C, compared to all other oscillators, with D-type failure occurring from 1.33 kV and E-type failure at 1.45 kV. The FD circuit plays a vital role in the case of the RO (operating frequency greater than 900 MHz), as lowering the temperature improved the performance of the FD and switched the output frequency to its expected value. When comparing the 3-stage CSVCO and RO at 120 °C, the latter's immunity was slightly lower (610 V (D) and 690 V (E)). The reason behind this is that the FD circuit is unable to function properly at elevated temperatures for the RO. Temperature variations did not influence the type of failure modes, and the D-type failure was still only noticed for the RO, due to the FD circuit.

The output peak voltage and input peak current of each oscillator at extreme temperatures were also examined and are given in Fig. 9a and 9b, respectively. Similarly to the results obtained at ambient temperature, the output peak voltage drops for all oscillators in the case of an E-type failure (Fig. 9a). The output peak voltages for increasing EFT injected voltage at −40 °C were substantially greater than at 120 °C for all oscillators. The maximal output peak voltages at −40 °C and 120 °C were obtained for the 3-stage RO (64.7 V) and 5-stage CSVCO (37.8 V), respectively.

As observed in Fig. 9b, the injected EFT input current was also reduced at elevated temperatures. At the lowest temperature, the largest EFT peak input current was noted for the 3-stage RO (12 A). However, at the maximum temperature, the highest peak input current was measured for the 3-stage CSVCO (5.9 A). Consequently, the 3-stages RO and CSVCO can withstand more injected EFT peak current than the 5-stage CSVCO at −40 °C and 120 °C, respectively.

The negative polarity EFT immunity levels of the packaged oscillators at nominal and extreme temperatures are illustrated in Fig. 10. As expected, the absolute EFT immunity levels were comparable with the positive polarity test (Fig. 8) and the overall trend with respect to thermal stress remained the same for all packaged tested oscillators. This is due to the

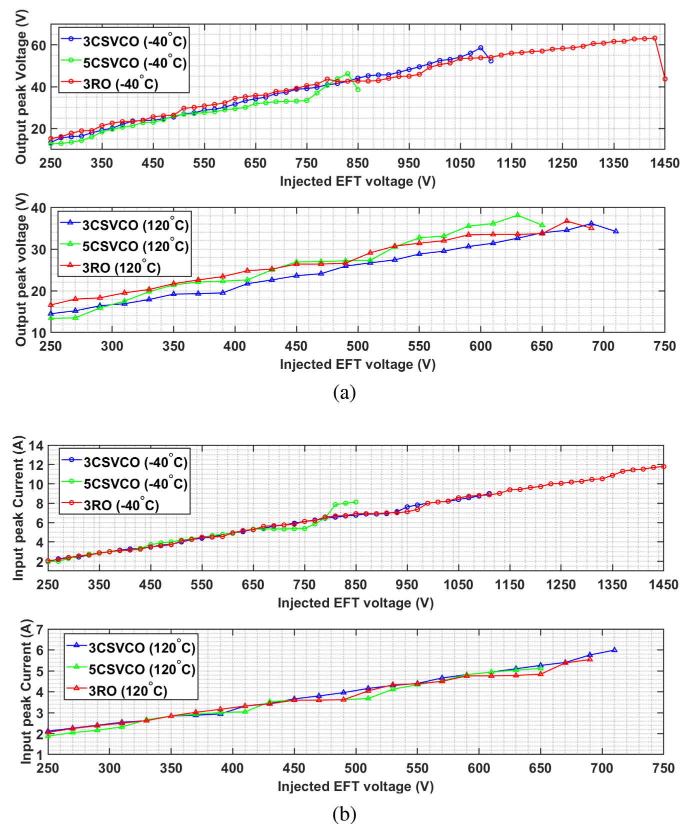


Fig. 9. Effect of EFT disturbances on multi-stage CSVCO and RO (packaged) at extreme temperatures: (a) output peak voltage; (b) input peak current.

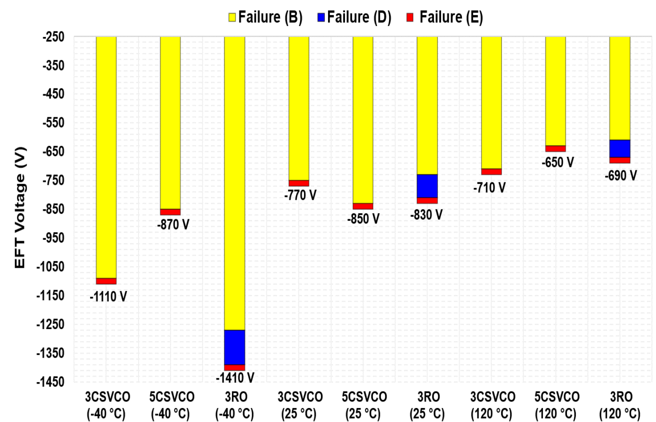
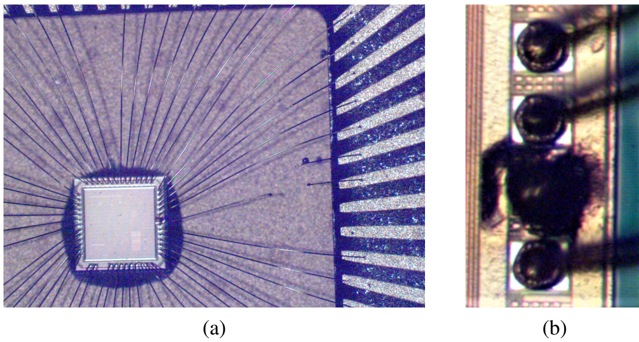


Fig. 10. Negative polarity EFT immunity of multi-stage CSVCO and RO (packaged) at nominal and extreme temperatures.

padring having identical ESD protection structures to both the supply rail and ground. Furthermore, changing the polarity did not have an impact on the EFT failure modes, as a D-type failure was still observed only for the 3-stage RO instigated by the FD circuit.

To physically demonstrate the destructive effect of EFT disturbances at the package and die level, a few images of the tested ICs were captured using a high resolution microscope (Leica MZ125). As an example, Fig. 11a and 11b show the packaged IC subjected to EFT at −40 °C at the bonding



(a) (b)

Fig. 11. Images of the damaged IC due to EFT disturbances at −40 °C: (a) bonding wire; (b) bond pad.

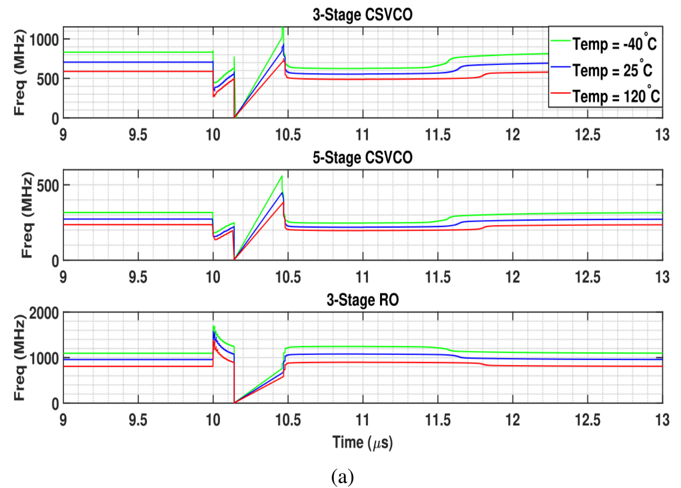
and die level, respectively. It can be noticed in Fig. 11a that two bonding wires, that were previously connected to the 3-stage CSVCO and RO voltage supply pads, were burnt. Both wires were damaged due to the overvoltage caused by the EFT disturbances, in this case being greater than 1.1 kV. However, only the voltage supply bondpad of the 3-stage RO was entirely destroyed (Fig. 11b). Therefore, the maximum EFT voltage that the ESD devices in the supply pads could handle was found to be 1.45 kV.

IV. Simulation Results and Discussion

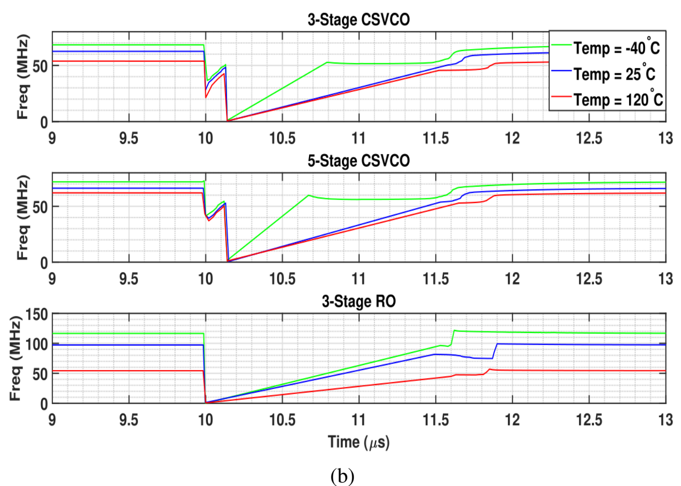
A. Simulation-based Frequency Response due to EFT Injection Under Thermal Stress

The simulation setup previously introduced in Section III-C was used to determine the frequency behavior of the considered oscillators before and after the FD circuit when subjected to EFT at nominal and extreme temperatures. The transient simulations were recorded for a time-period of 13 μs in order to monitor the oscillator frequency deviation due to one EFT spike. It was verified that the EFT disturbance (600 V) was injected when all tested oscillators' output signals were in-phase (rising edge) at 10 μs whatever the temperature, in order to draw a sensible comparison among all transient effects (Fig. 12a and 12b). The Cadence SKILL mode function, which takes the fast Fourier transform in discrete time-steps (1.5 ns) over the steady-state period (13 μs), was applied to measure the operating and output frequency of the oscillators.

As illustrated in Fig. 12a, excluding the effect of the FD and output pad, an identical frequency response to EFT injection was observed for the considered multi-stage CSVCOs. However, the 3-stage RO exhibited a distinct operating frequency behavior, which is likely to be due to the topologies of the CSVCO and RO. At 10 μs, when the EFT disturbance is injected into the supply V_{DDI} pad, the ESD structures are triggered after 100 ns, clamping the EFT voltage to 0 V. Before that clamping, the increase in supply voltage reduces the propagation time of the RO's inverter stages, thus momentarily increasing its frequency. Conversely, for the CSVCOs, the EFT spike is capacitively coupled to the gate of the PMOS biasing transistors, resulting in a reduction of the bias current, which in turn increases the propagation delay and reduces the output frequency. Both phenomena tend to stabilize before the ESD structures are triggered.



(a)



(b)

Fig. 12. Frequency variation of multi-stage CSVCO and RO (packaged) at extreme temperatures before (a) and after (b) the FD circuit when an EFT voltage of 600 V is applied.

After 100 ns, when all the oscillators start recovering to their nominal frequency, the CSVCO has a faster slew rate compared to the RO (Fig. 12a). However, unlike the RO where it smoothly stabilizes to its nominal frequency, the CSVCO frequency sharply increases and then falls down due to the discharge of the parasitic gate-source capacitances of the CSVCO's PMOS bias transistors (verified in simulations). Moreover, it was observed that with the rise in temperature, the time to recover after the EFT injection gradually increased for all oscillators due to the higher peak voltages.

For a better understanding of the measured results, the frequency response of all tested oscillators, including the effect of the FD, output pad and package, was further analyzed in simulations (Fig. 12b). At 10 μs, when the EFT disturbance is injected, the CSVCOs exhibit similar behavior to the case before the FD, where the output frequency momentarily reduces before being clamped to ground by the ESD structures. After 100 ns, compared to the former case, the frequency tends to stabilize but with a reduced slew rate due to the added effect of the FD. The latter also explains the difference in the simulated slew rate at extreme temperatures.

Conversely, in the case of the RO, once the EFT is applied,

the output frequency abruptly drops to 0 Hz. The latter is attributed to the fact that the RO is operating (955 MHz) above the maximum clock frequency of the FD (900 MHz) and a further increase in the RO frequency results in the FD circuit crashing at 10 μs. It gradually tries to recover to its nominal output frequency but with a lower slew rate compared to the CSVCOs, which is due to the higher propagation delay caused by the FD circuit. Similar to the CSVCO, the slew rate is observed to be inversely proportional to temperature.

To sum up, temperature variations do not impose any change in the transient latch-up mechanism of the ESD structures, which explains the unchanged behavior in the output frequency curves for all oscillators before the FD. A rise in temperature only accounts for the decrease in the nominal operating frequency (Fig. 12a) and a reduction in the slew rate of the output frequency (Fig. 12b) for all tested oscillators. The simulated operating frequency deviations from the nominal frequency for the 3- and 5-stage CSVCO and 3-stage RO (before the FD) at extreme temperatures are +15.1%, +14.3%, +15.6% (at −40 °C), and −16.7%, −13.2%, −17.4% (at 120 °C), respectively. The output frequency deviations (after the FD) at extreme temperatures are in line to those obtained in measurements (Section II-B), with the 3-stage RO showing the highest deviation due to the added effect of the FD circuit.

Consequently, the 5-stage CSVCO was found to be the most resilient to temperature variations compared to the other two oscillators mainly due to the reason previously explained in the last paragraph of Section II-B. However, the 5-stage CSVCO was the most susceptible to the combined effect of temperature and EFT injection. The latter and the root cause of failure will be verified through further simulations and reported in the upcoming section.

B. Failure Analysis Due to EFT Injection Under Thermal Stress

To investigate the root cause of the EFT susceptibility of the oscillators at extreme temperatures, a transient simulation was carried out for the EFT disturbance (600 V) peak by varying the temperature from −40 °C to 120 °C with a 20 °C step size. Relevant MOSFET characteristics such as peak drain current, on-state drain-to-source resistance and power dissipation were calculated at the output stage (before the FD circuit) of the considered oscillators as a function of temperature (Fig. 13).

As observed in Fig. 13a, the peak drain current in the inverter output stage reduces with the increase in temperature for all the tested oscillators even when subjected to EFT disturbance. This is due to the μ_{eff} of the MOSFETs being inversely proportional to temperature. The multi-stage CSVCOs have a lower drain current than the RO since the biasing MOSFETs limits the current to the inverter stage. When comparing the 3- and 5-stage CSVCOs, the former has higher peak drain current because of different external biasing voltages. It is noted that the 3-stage RO's peak drain current is more resilient to changes in temperature in comparison to the multi-stage CSVCOs. A reasonable explanation for this observation can be found by analyzing the on-state drain-to-source resistance of the output stage (Fig. 13b).

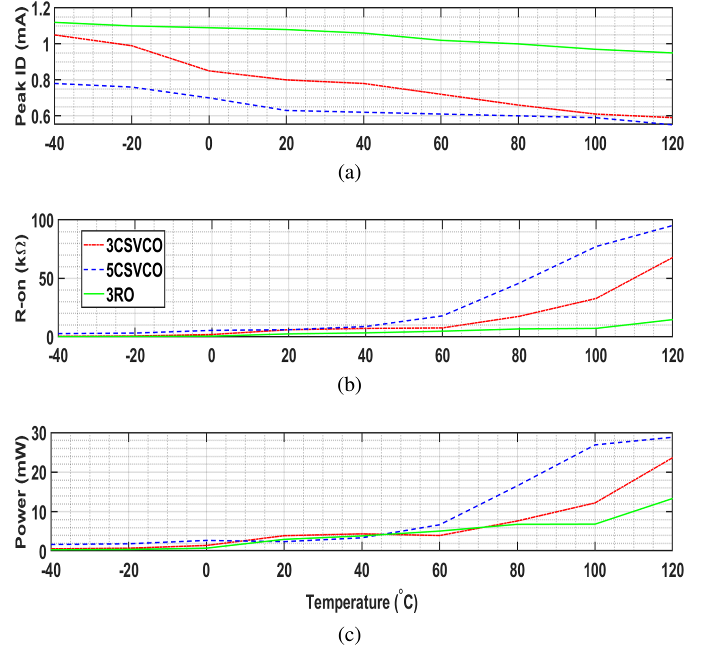


Fig. 13. Dependency of the relevant MOSFET characteristics of multi-stage CSVCO and RO (packaged) as a function of temperature for an EFT applied voltage of 600 V: (a) peak drain current; (b) on-state resistance; (c) power dissipation.

Temperature variation and transient electrical overstress such as EFT cause the on-state resistance of the MOSFETs in the inverter stage of oscillators to substantially increase. The on-state resistance rises due to the reduction in μ_{eff} and V_{th} with the combined effect of temperature and EFT. These changes cause the switching characteristics of the oscillator to change, resulting in higher power dissipation and causing premature failure [31].

When the EFT disturbance is injected into the V_{DDI} of each oscillator, a transient path is created between V_{DDI} and G_{NDI}. Hence, the total on-state resistance of each oscillator is calculated by the summation of the individual on-state resistance of each P-MOS and N-MOS in the output branch with temperature variations. As illustrated in Fig. 13b, the on-state resistance of the multi-stage CSVCOs is greater than the RO due to the added resistance of the biasing MOSFETs. For the former, the total on-state resistance abruptly rises above 60 °C. When comparing the 3- and 5-stage CSVCOs, the latter has an elevated resistance over the entire temperature range, which is due to the combined effect of lower μ_{eff} and V_{th}, elevating the on-state resistance when EFT is applied. In contrast, the 3-stage RO has a lower variation in the on-state resistance to temperature and EFT stress.

All the analyzed characteristics are directly influenced by the decrease of the μ_{eff} and V_{th} levels of the MOSFETs due to rise in temperature and EFT stress. For example, the behavior of these characteristics for a P-MOS in the inverter output stage as a function of temperature for all tested oscillators is illustrated in Fig. 14a and 14b, respectively. The μ_{eff} of the 5-stage CSVCO was found to be the least resilient to the combined effect of temperature and EFT; it drops sharply for temperatures above 80 °C. In comparison,

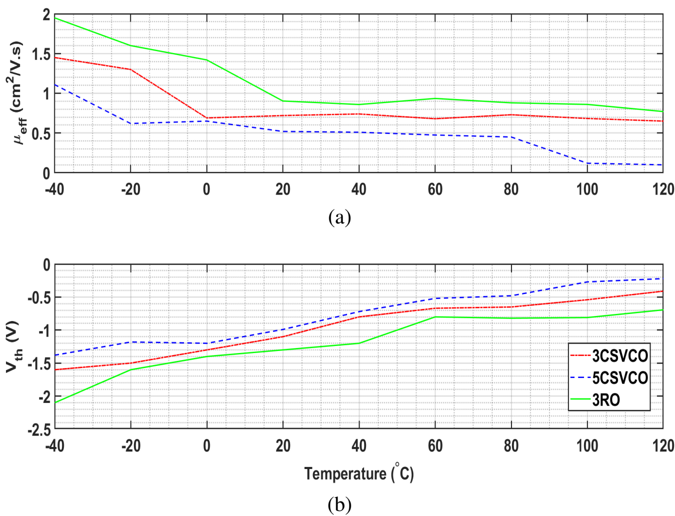


Fig. 14. P-MOS relevant characteristics in the inverter output stage of multi-stage CSVCO and RO (packaged) as a function of temperature for an EFT applied voltage of 600 V: (a) μ_{eff}; (b) V_{th}.

the 3-stage CSVCO and RO have limited reduction in μ_{eff}. Moreover, the absolute V_{th} levels of the 5-stage CSVCO are also lower than the other oscillators over the entire temperature range. The root cause for the lowest EFT immunity of the 5-stage CSVCO is the increase on-state resistance due to the above-mentioned factors.

The power dissipated at the output stage of all oscillators is derived from the peak drain current and the on-state resistance. As displayed in Fig. 13c, the power dissipation follows a similar trend and is influenced more by the on-state resistance and increases at elevated temperatures for all oscillators. The maximum power dissipation is observed at 120 °C for the 3-stage (23 mW), 5-stage (29 mW) CSVCO and 3-stage RO (14 mW). It is important to note that when the EFT is applied at nominal temperature, the 5-stage CSVCO has a reduced power dissipation (2.4 mW) compared to the 3-stage CSVCO (3.9 mW) and the 3-stage RO (3.1 mW). Although the self-heating phenomenon due to that power dissipation is not taken into account by the simulator, that may explain why E-type failures can be observed in measurements due to thermal runaway.

V. CONCLUSION

The transient immunity of three multi-stage SOI integrated oscillators, i.e. CSVCO and RO, having the same ESD protection structures, was assessed under EFT and thermal stresses. By considering output frequency as the failure criterion, EFT failure modes were proposed for such oscillators. Depending on oscillator topology, distinct failure modes occurred; B- and E-type were observed for all the considered oscillators, whereas a D-type failure was only noticed for the RO mainly due to the frequency limitation of the FD circuit. Moreover, the analysis revealed the importance of the package on the EFT immunity levels of all the tested oscillators, due to the attenuation of the injected EFT peak voltage.

Transistor level simulations were also conducted to accurately monitor the output frequency response of each oscillator to EFT injection under thermal stress, with and without the effect of the FD, the analog output pad and the package. A distinct behavior in oscillator frequency was observed for the same in-phase EFT injections depending on the topology of the circuit. The FD circuit causes an overall reduction in the slew rate and increases the recovery times of each oscillator after EFT disturbance is applied. Additionally, temperature elevation was found to decrease the output frequency of each oscillator while the transient latch-up behavior of the ESD devices remained unaffected.

The positive and negative polarity EFT immunity levels for all tested oscillators were found to be similar since the IC's padring includes the same ESD protection circuits to the supply and ground. The rise in temperature was demonstrated to reduce the absolute EFT immunity levels for all the tested oscillators by affecting the protection capability of the ESD devices. The 5-stage CSVCO was found to be the most resilient to temperature variations when compared to the other two oscillators. However, the results were entirely different when the oscillators were subjected to the combined EFT and temperature stresses. The 5-stage CSVCO was found to be the most susceptible to EFT at extreme temperatures (−40 °C and 120 °C). Conversely, at the minimum and maximum temperatures, the 3-stage RO and CSVCO were shown to be the most immune to EFT, respectively. The temperature variation under the EFT stress resulted in no impact on the type of failure modes.

The output inverter stage MOSFET characteristics such as drain currents, on-state drain-to-source resistance, power dissipation, μ_{eff} and V_{th} were extensively analyzed while varying temperature and EFT stress. The on-state resistance of the MOSFETs varies considerably when EFT stress and temperature variations are combined. The root cause for the latter is the combined reduction of μ_{eff} and absolute V_{th} levels with EFT stress at extreme temperatures. This leads to enhanced power dissipation, which may damage the oscillator by thermal runaway particularly for the 5-stage CSVCO.

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Qazi Mashaal Khan (Graduate Student Member, IEEE) received the Bachelor's degree in Electrical Engineering from FAST NUCES university, Pakistan, in 2016, with summa cum laude. He finished the Joint Master's Degree in Smart Systems Integration with distinction in 2019. This was an EU funded Erasmus + Program where he spent his four semesters in UK, Norway, Hungary and Germany. The host was Heriot-Watt University, UK. He is currently working towards his Ph.D. research at the Radio and Hyper-frequency (RF) and the Electromagnetic Compatibility (EMC) group at ESEO, France. As part of the MSCA ETN PETER, he will carry out the extension of the IC Immunity and Emission models to incorporate environmental stresses. His Doctoral Degree will be provided by INSA Rennes University. His research interests include ageing, thermal stresses and obsolescence on EMC behavior on many categories of ICs.

Mohsen Koohestani (Senior Member, IEEE) received the PhD degree (Hons.) in electromagnetics from the école polytechnique fédérale de Lausanne (EPFL), Lausanne, Switzerland, and the Universidade de Lisboa (ULISBOA), Lisbon, Portugal, in 2014.

From 2014 to 2018, he was a senior research fellow with the Institut d'Electronique et de Télécommunications de Rennes (IETR), University of Rennes 1, working mainly on biomedical applications of wireless power transfer systems. He is presently an Associate professor at ESEO School of Engineering, Angers, France (since 2018). He is also an associate researcher at IETR, UMR CNRS 6164. He has authored over 70 peer-reviewed scientific papers. His main interests lie in the domain of antennas, microwaves, EMC, and biomedical engineering.

Dr. Koohestani is an official member of the IEC standardization working group (WG2 & WG9) in the SC47A French subcommittee on the EMC for integrated circuits.

Richard Perdriau (Senior Member, IEEE) was born in Angers, France, in 1971. He received the engineering degree in electronics and computer science from ESEO Angers - Grande Ecole d'Ingénieurs Généralistes, Angers, France, in 1992, the Ph.D. degree in applied sciences from Université Catholique de Louvain, Louvain-la-Neuve, Belgium, in 2004, and the "Habilitation à Diriger des Recherches" (Accreditation Degree) from Université de Rennes 1, Rennes, France, in 2012.

From 1992 to 2012, he was an Associate Professor with ESEO School of Engineering in the fields of microelectronics and embedded systems. In 2013, he became a Full Professor. His research interests include EMC of integrated circuits, mixed-signal hardware description languages, and integrated circuit design. Dr. Perdriau served as the Vice-Chair and the Technical Program Co-Chair of EMC Europe 2017. In January 2020, he was elected as the Secretary of the IEEE France Section.